Sigma-Delta modulator

ECE262 Project Report
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Contents

Introduction

1.1 Project Function

In this project, we built a Sigma Delta modulator. The most striking feature of a sigma delta modulator, which is the main component of sigma delta ADCs, is that these modulators use a very high sampling rate. The sampling rate used is in the range of MHz, which is much higher than the Nyquist rate, generally in the range of kHz. Hence, the oversampling ratio is very high, because of which these are sometimes referred to as oversampling ADCs. The advantage of using this very high sampling ratio is high resolution of the digital output and better noise shaping.

The main components of a sigma delta modulator are: a summer, an integrator, a comparator, a D flip-flop and a DAC. The difference of the analog input and the output of the modulator, fed back to the input through a DAC, is fed to the integrator. The integrator ramps up or down depending upon whether the difference being fed is positive or negative. The output of the integrator goes into a comparator. The comparator produces 5V or 0V depending on whether the output of the integrator is above or below the threshold voltage being compared by the comparator. The comparator's output is fed to a D Flip-flop which operates at a very high frequency (~MHz), which in turn connects to a DAC. The output of this DAC is fed to the summer at the input stage. For our project, we omitted the DAC, and instead used a resistor-divider circuit after the D Flip-flop to make sure that the input being fed back into the summer is within the appropriate range. Thus, the main components for our project were:

- Summer
- Integrator
- Comparator
- D Flip-flop

To arrange four components in the floor-plan, we make each component as below. Besides, Since integrator includes a large capacitance and a large resistance. We make them off-chip.

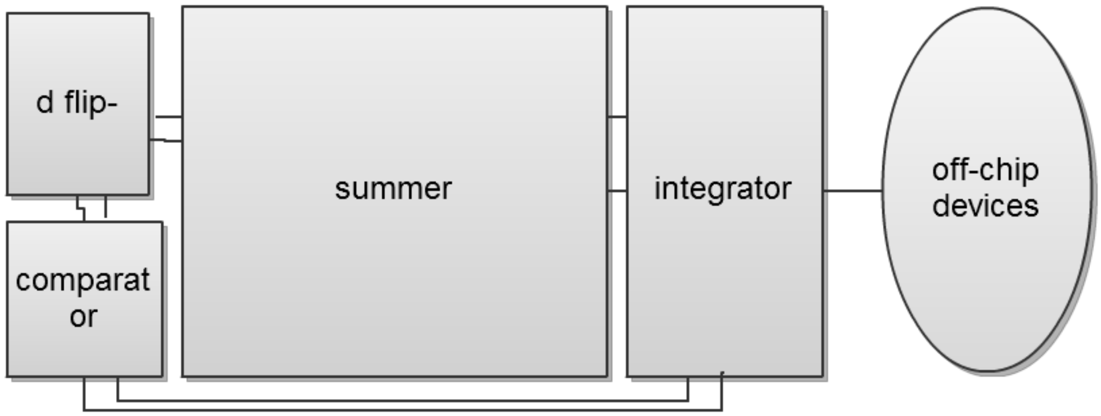


Figure 1 Sigma delta modulator floorplan

1.2 System Verification Simulation

In the mean time, we make block diagram of this sigma-delta modulator in Matlab/Simulink. And simulate the sigma-delta modulator using digital simplified method to verify the functionality of the device. Block diagram of sigma-delta is shown below,

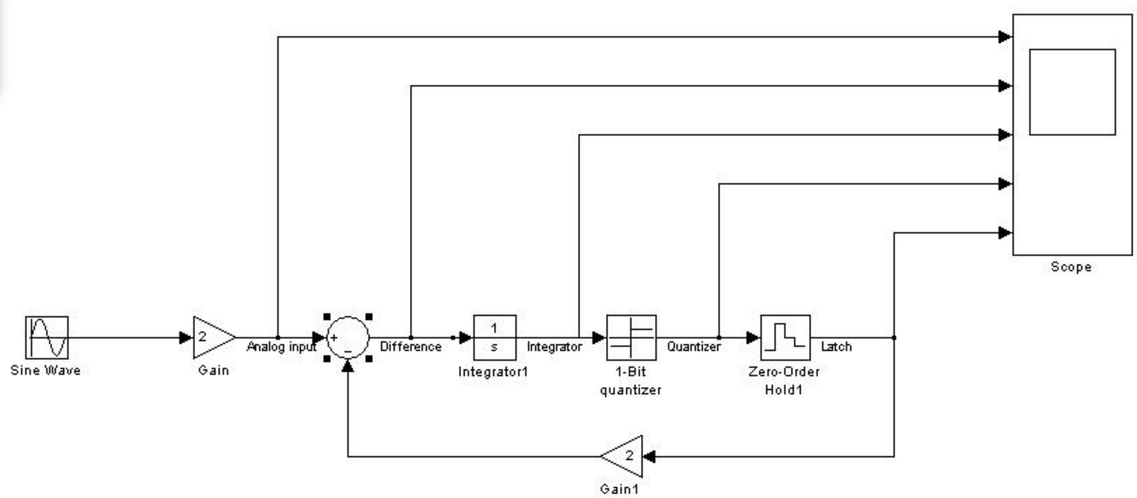


Figure 2 Sigma Delta modulator Matlab/Simulink model

In each stage, we can get different output. First we add up the original signal and negative adjusted pulse output of dff. After we integrate the difference of this stage, and quantize the result. We get result of 0 and 1 output signal representing a sinusoidal waveform. We get more 0/1 oscillation in the center of input range; and we could get more 1 when input is high, otherwise more 0 when input is low.

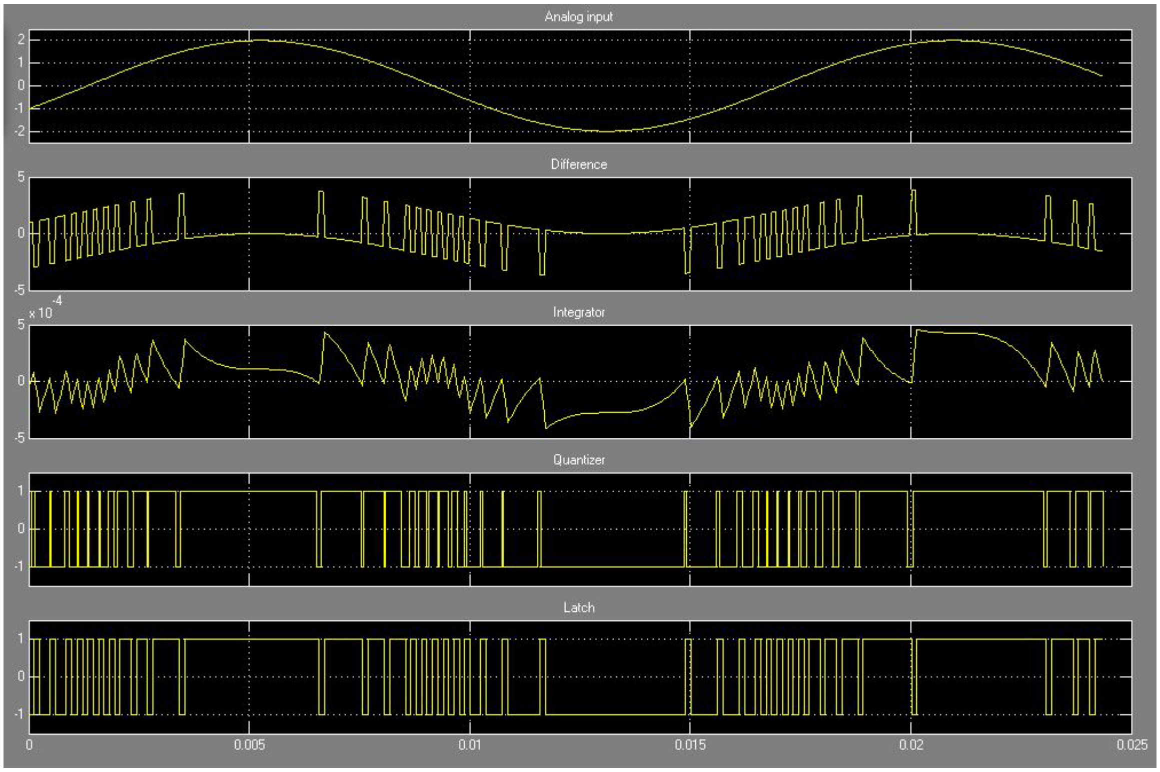


Fig 3 each stage output of Sigma delta modulator

1.3 Performance Estimation

Total number of transistors used: 39.
Total power consumption: 12.2573 mW
Total area of the circuit: 864 um* 340 um = 0.29mm^2
besides we need a 1uf off-chip capacitance and a 20 Meg Ω off-chip resistance
Sampling frequency: 2.5 MHz
Input Signal frequency: 2kHz
These components are discussed in detail in the following chapter.

Sub-circuit Design

The whole system consists of a summer, an integrator, a comparator and a d flip-flop. Below, we will discuss each component by its function, simulation verification, schematic and its layout.

2.1 Summer

The summer was simulated using HSpice, and was found to function correctly. Its output range was 1.5V to 5V. Below 1.5V, distortion occurs and above 5V, clipping occurs. The simulation results for the summer are shown below. The first simulation was done using a DC voltage as the 1st input to the summer and pulse as the 2nd input. The value of the DC voltage was 1V and the pulse low and high values were 0V and 1V respectively. The output of the summer in this case was a pulse varying from 1.5V to 2.5V. This is shown in figure 1. The second test on the summer was done using a DC voltage of 1V as 1st input, and a sine wave with amplitude of 1V and centered at 2.5V as the 2nd input. The result, in this case, was a sine wave centered at 3.5V, and having amplitude of 1V. This is shown in figure 2. The schematic and layout for the summer are shown in Figures 3 and 4 respectively.

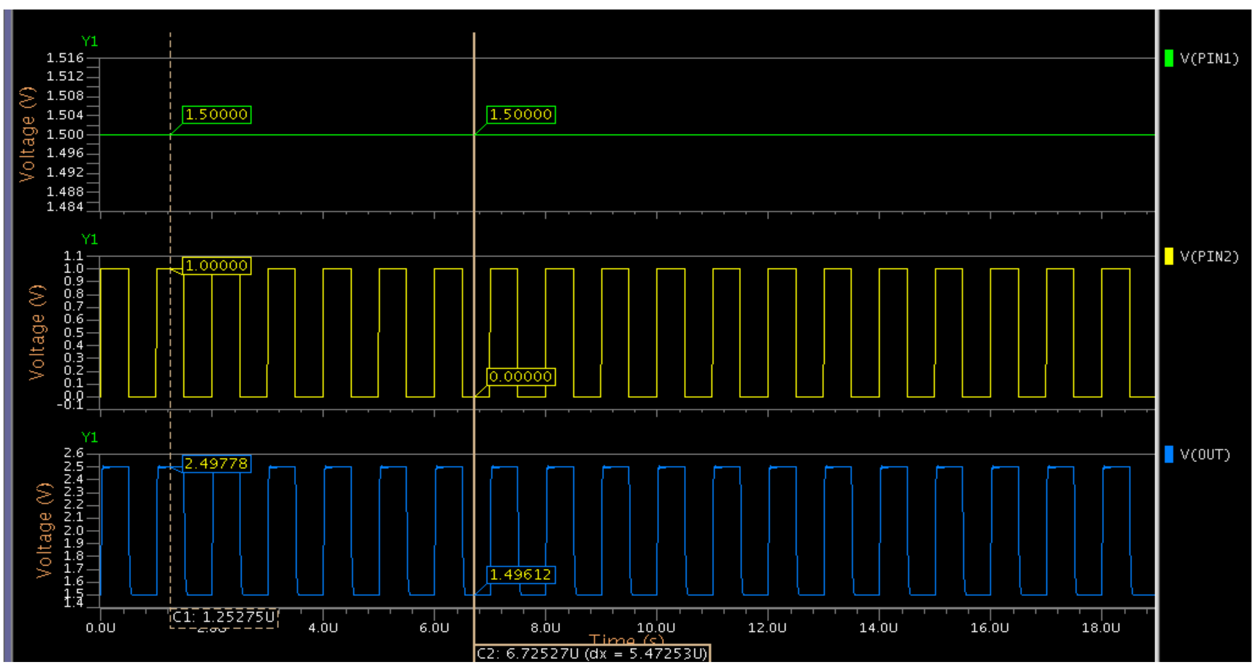


Figure 4: Output of Summer for a DC voltage of 1.5V and a pulse varying from 0V to 1V

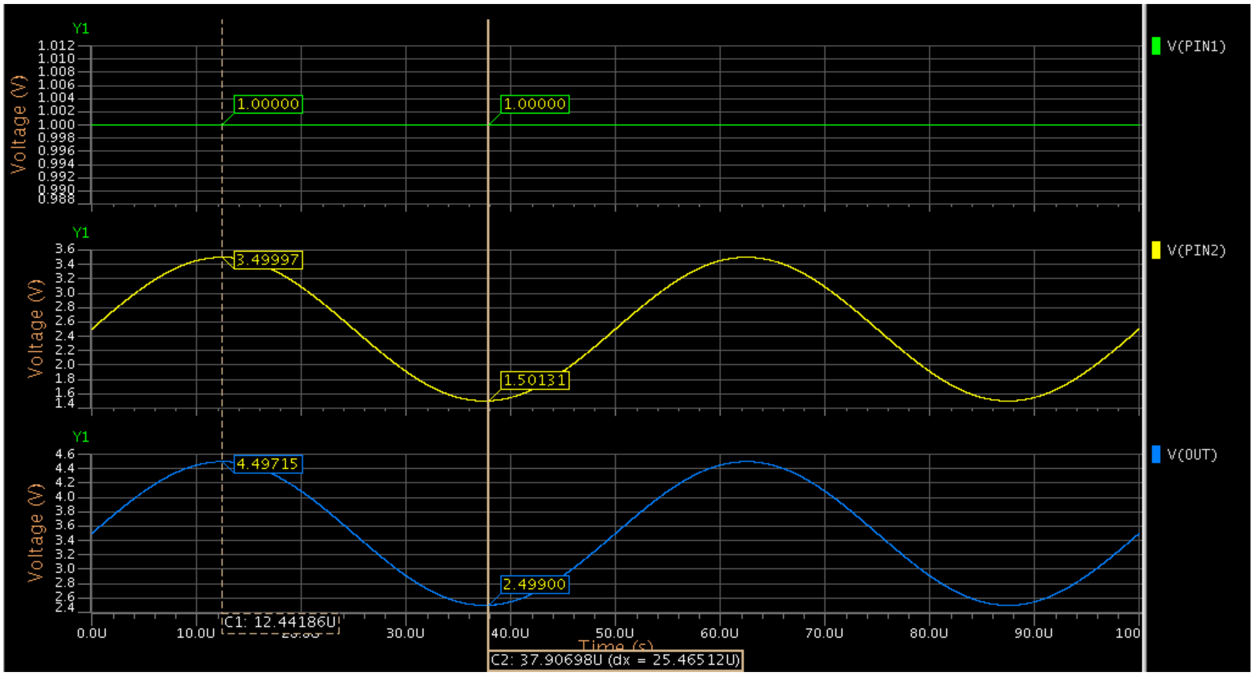


Figure 4: Output of Summer for a DC voltage of 1V and a sine wave of 1V centered at 2.5V

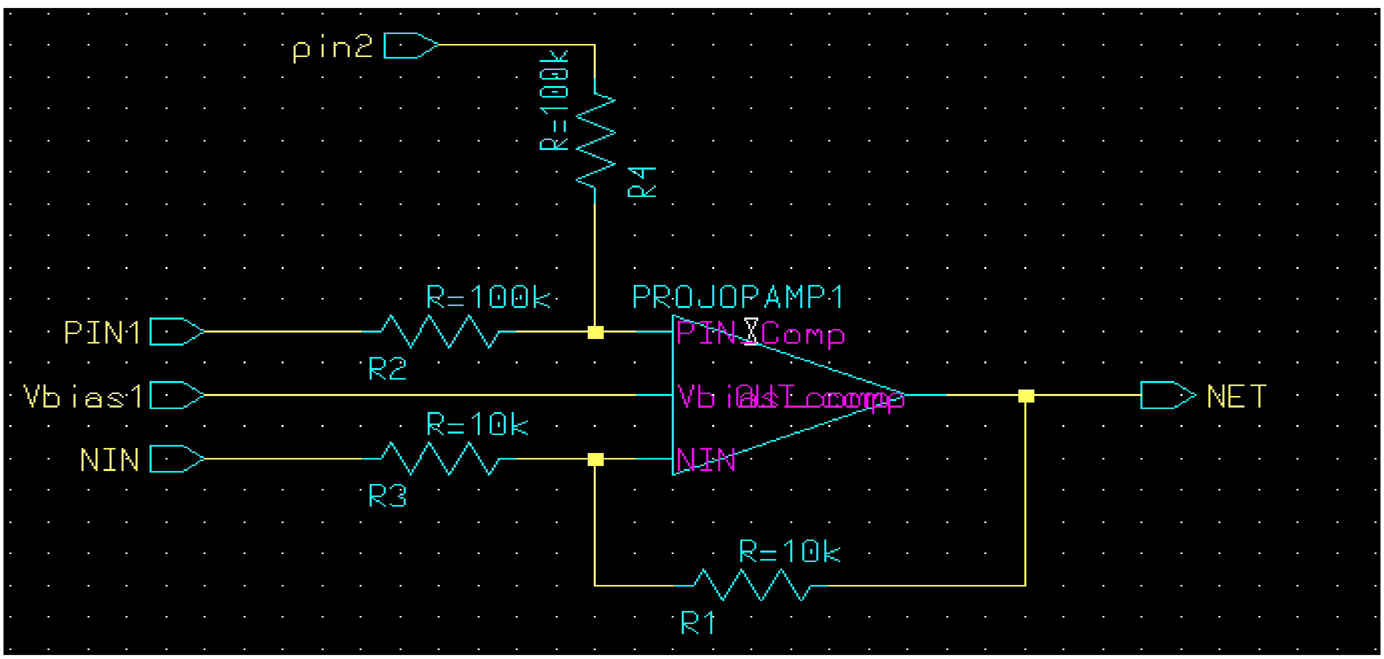


Figure 5: Schematic for Summer

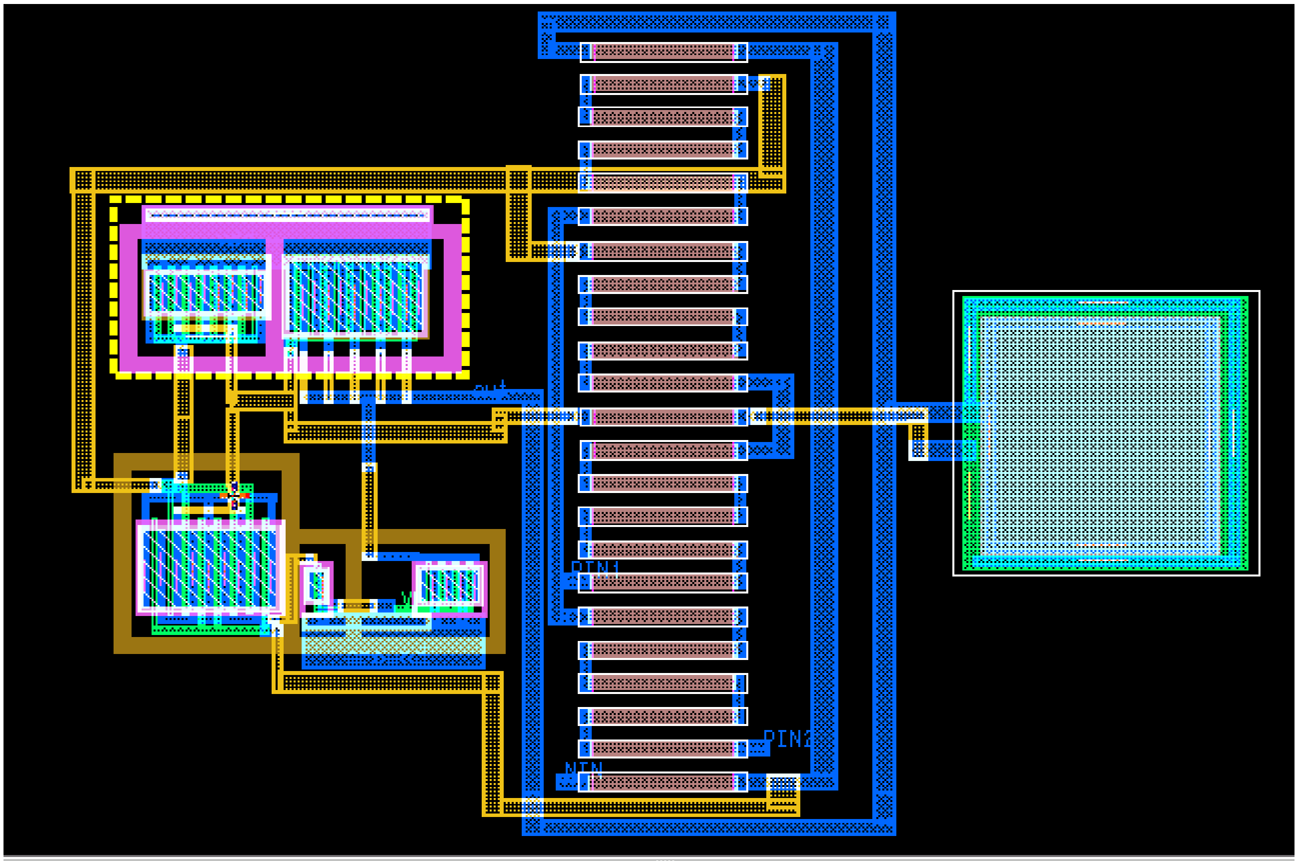


Figure 6: Layout of Summer

2.2 *Integrator*

The integrator used a high capacitance of 1u to make its working robust. It was tested using both, a DC input voltage, in which case the output was a ramp, and a pulse input, in which case the output was ramping up or down depending upon whether the input was higher or lower than 2.5V. The integrator was centered at 2.5V. Since the capacitance used was very large, therefore, in the layout, this capacitor was kept as an off-chip component. The simulation results are shown in Figures 5 and 6 below.

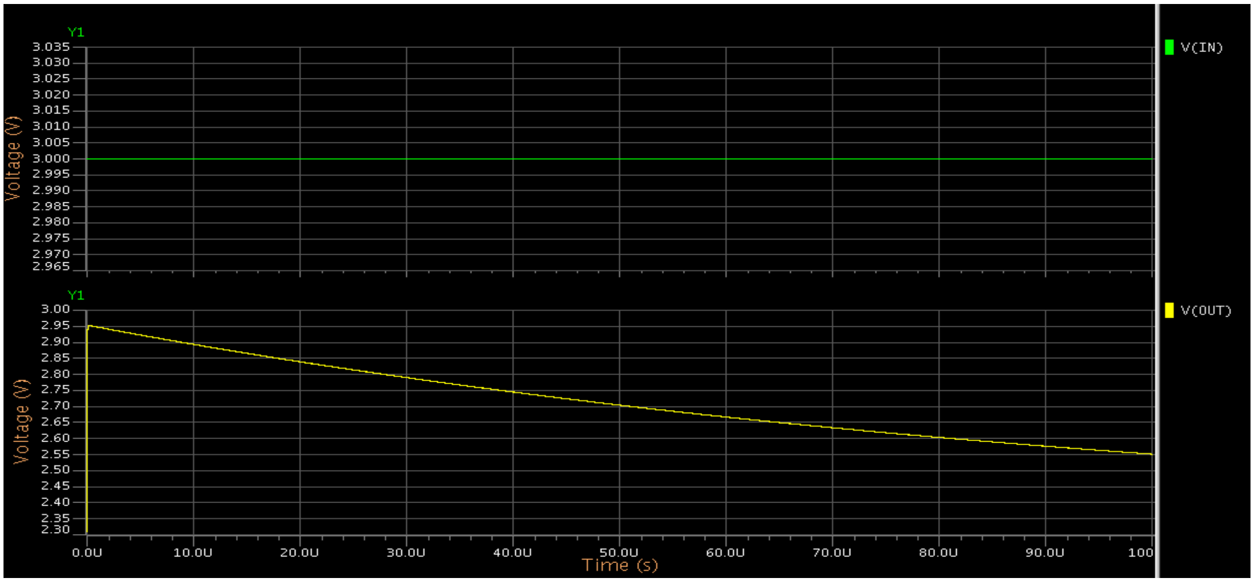


Figure 7: Output of Integrator for a constant DC input of 3V

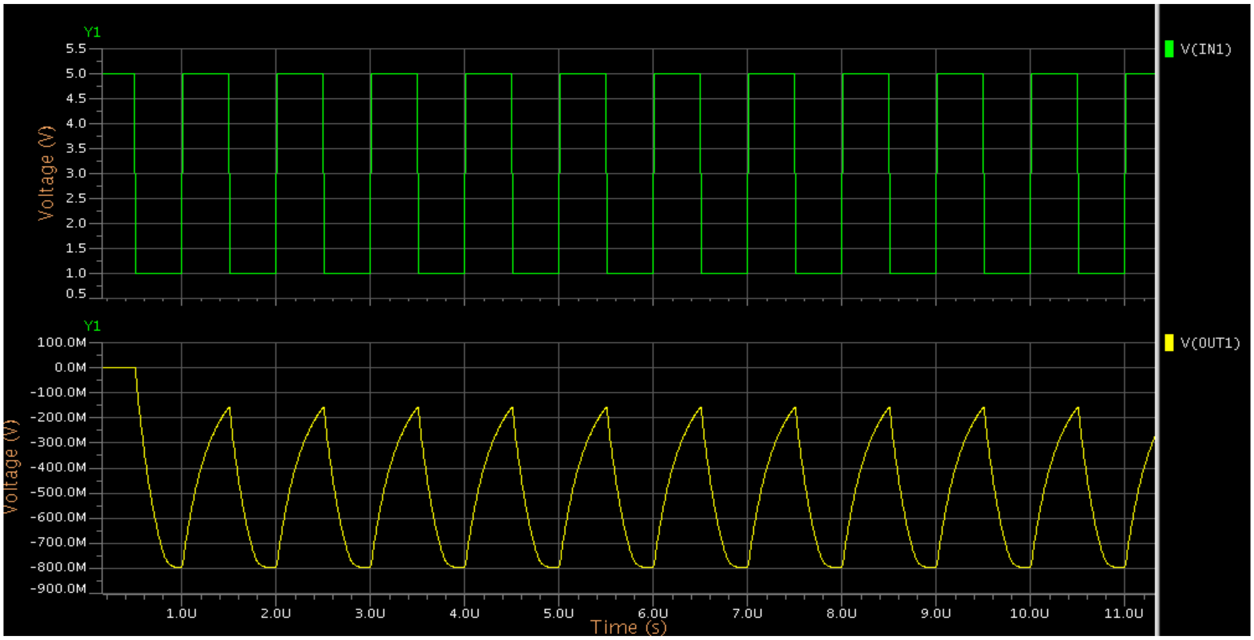


Figure 8: Output of Integrator for a pulse input

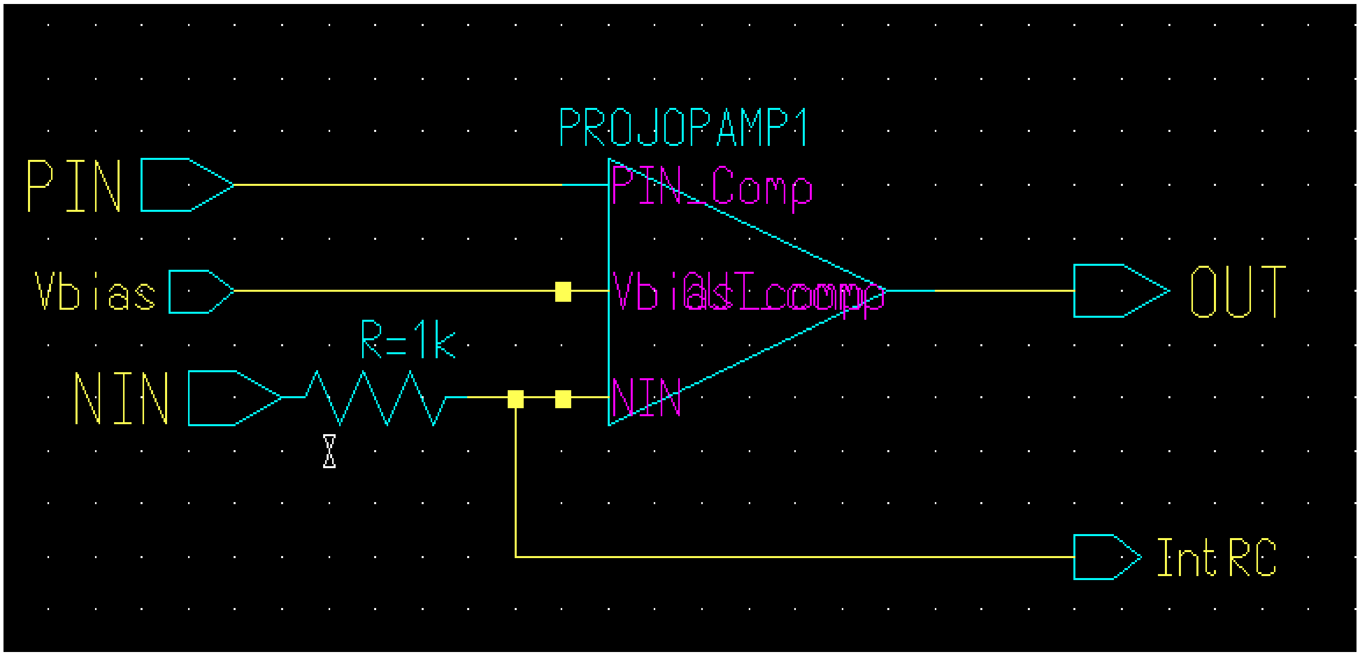


Figure 9: Schematic for Integrator (off chip capacitance of 1uF connected between IntRC & OUT)

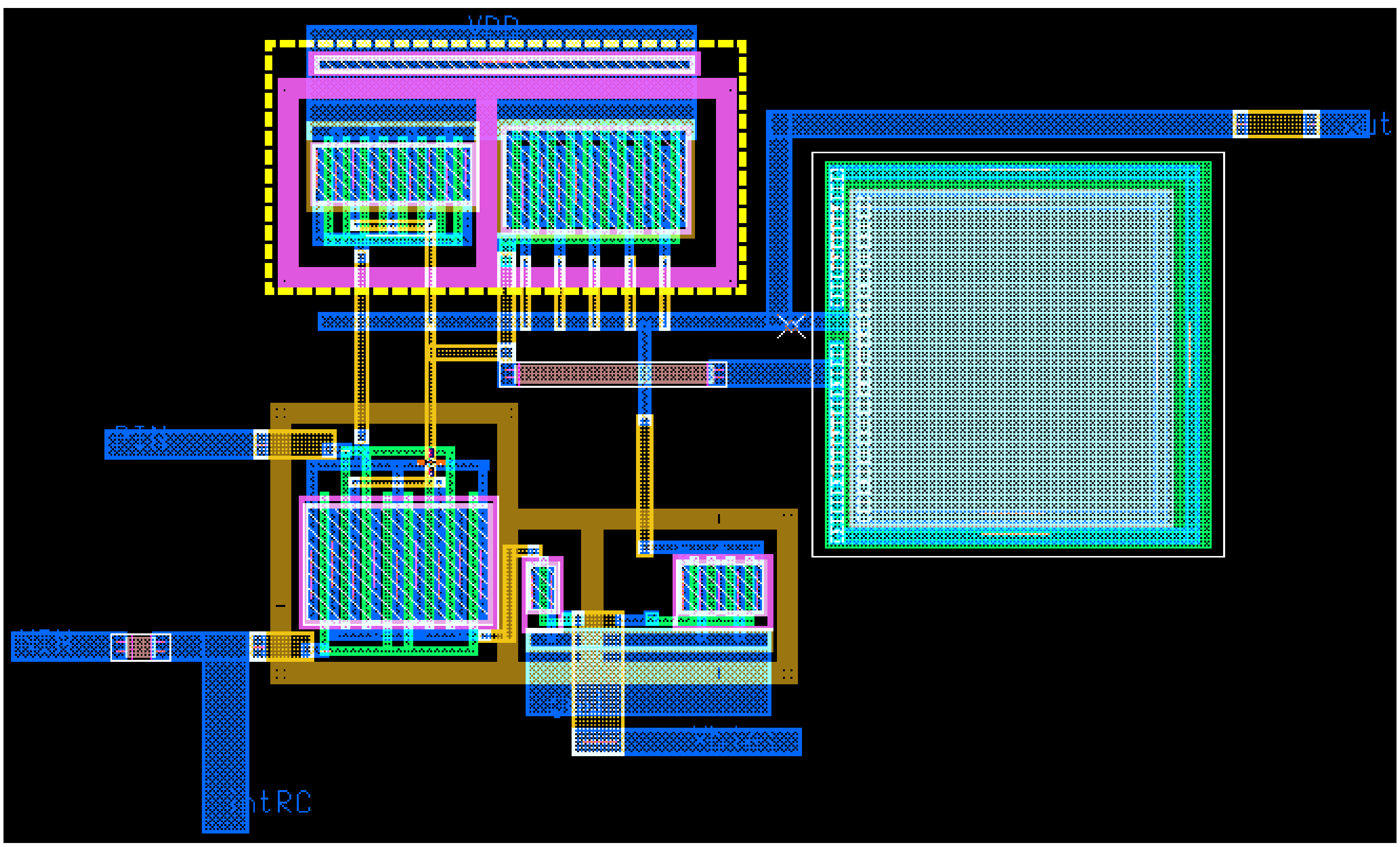


Figure 10: Layout of Integrator

2.3 Comparator

The comparator was also centered at 2.5V. Thus for input voltage higher than 2.5V, the output was 5V, and for input voltage lower than 2.5V, the output was 0V. The simulation results are shown in Figure 9.

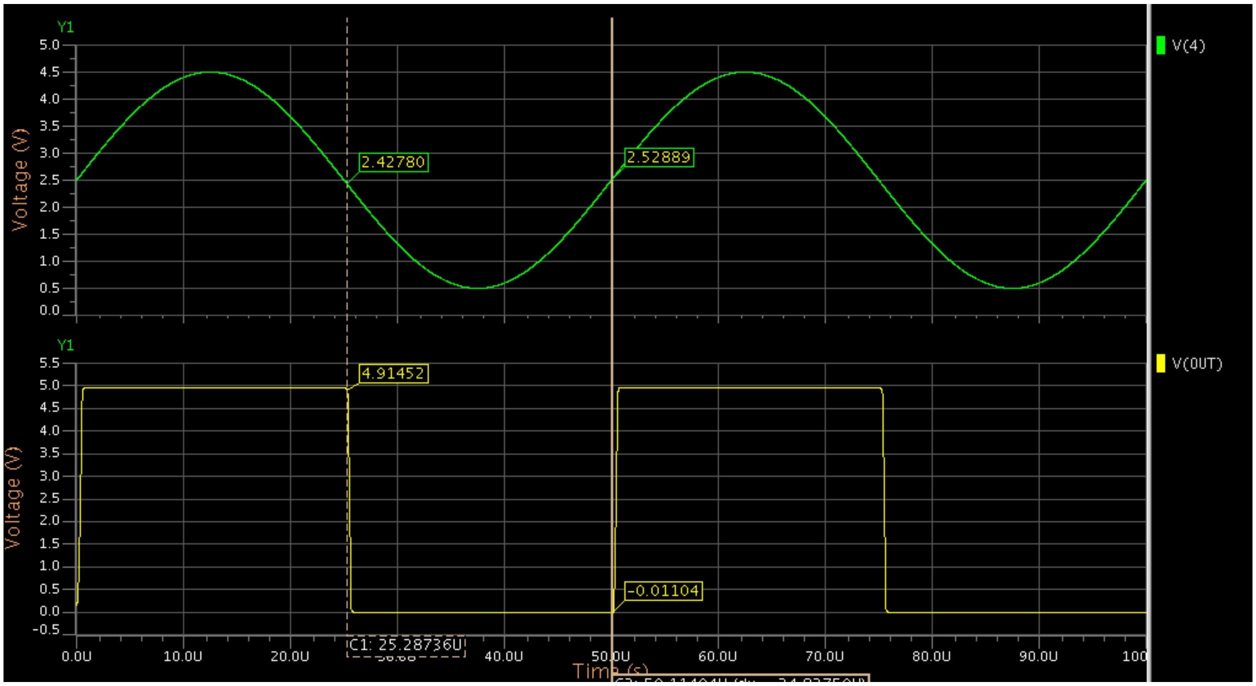


Figure 11: Output of Comparator (threshold voltage is 2.5V)

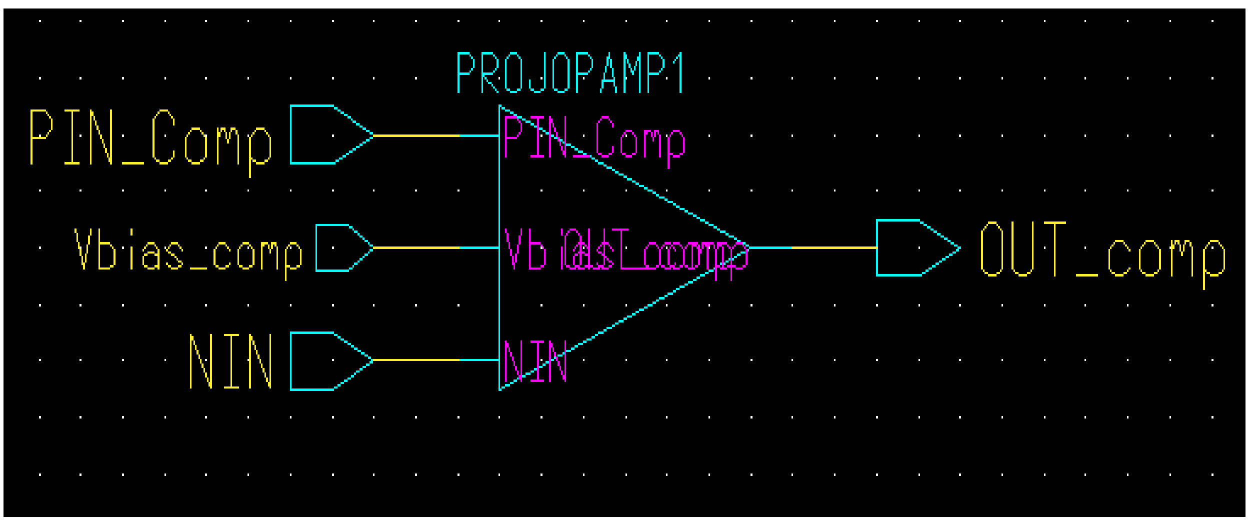


Figure 12: Comparator Schematic (PIN_Comp is connected to 2.5V which is the threshold and the input signal being compared is connected to NIN)

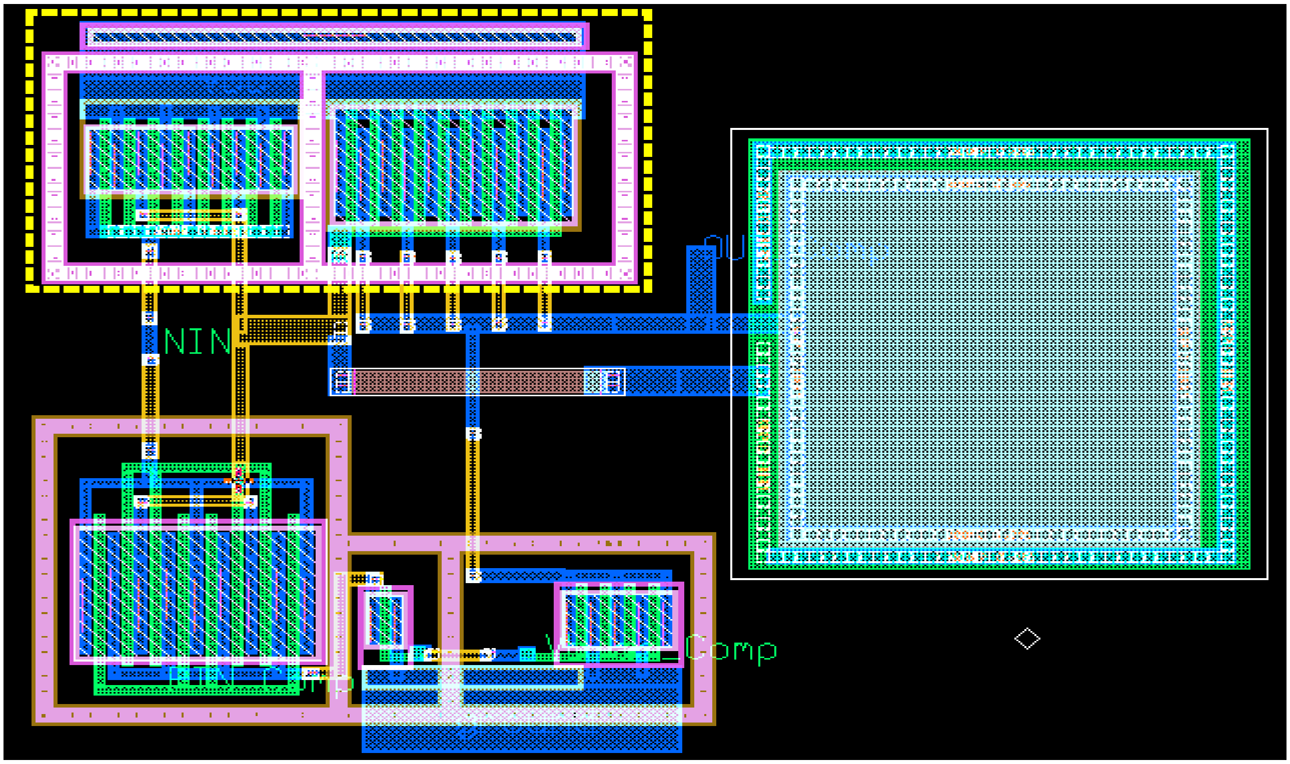


Figure 13: Comparator Layout

2.4 D Flip-flop

This is the only digital component in our system. It was simulated using HSpice and was found to function correctly. The simulation results are shown in Figure 12. Following the simulation results, the schematic and layout for the D Flip-flop are shown. Both the D Flipflop and the whole of the analog section of the circuit were surrounded by guard rings to ensure that these parts are isolated from each other. The Qbar output of the D Flipflop was made to pass through a resistor-divider circuit and then fed back as the 2nd input of the summer.

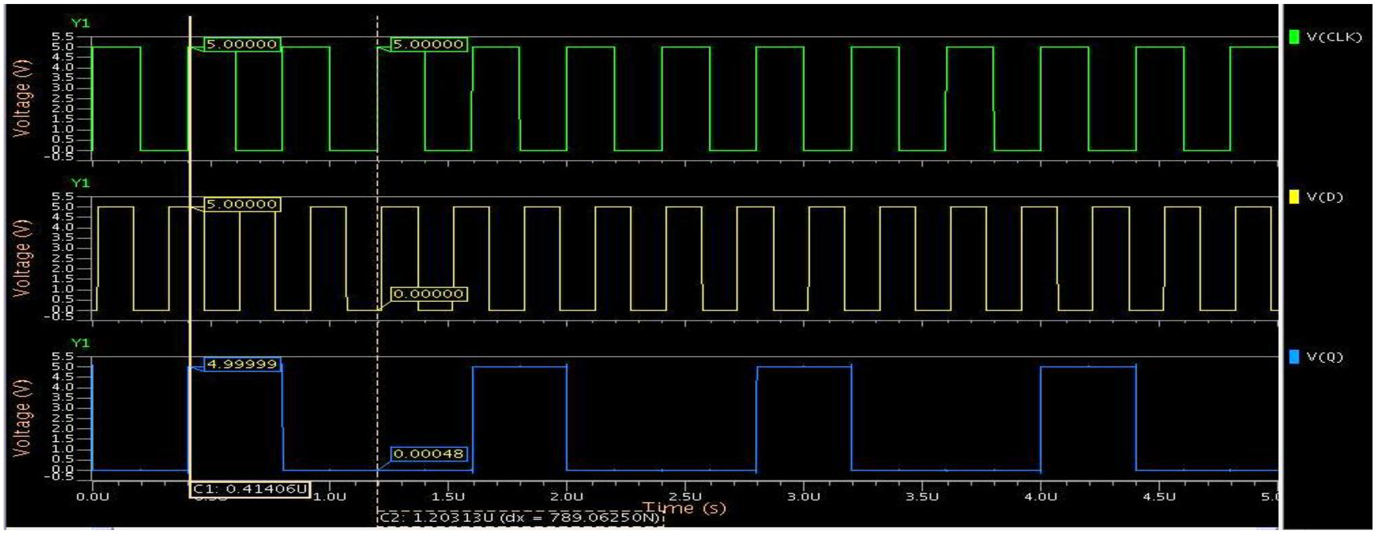


Figure 14: Simulation result for D Flipflop

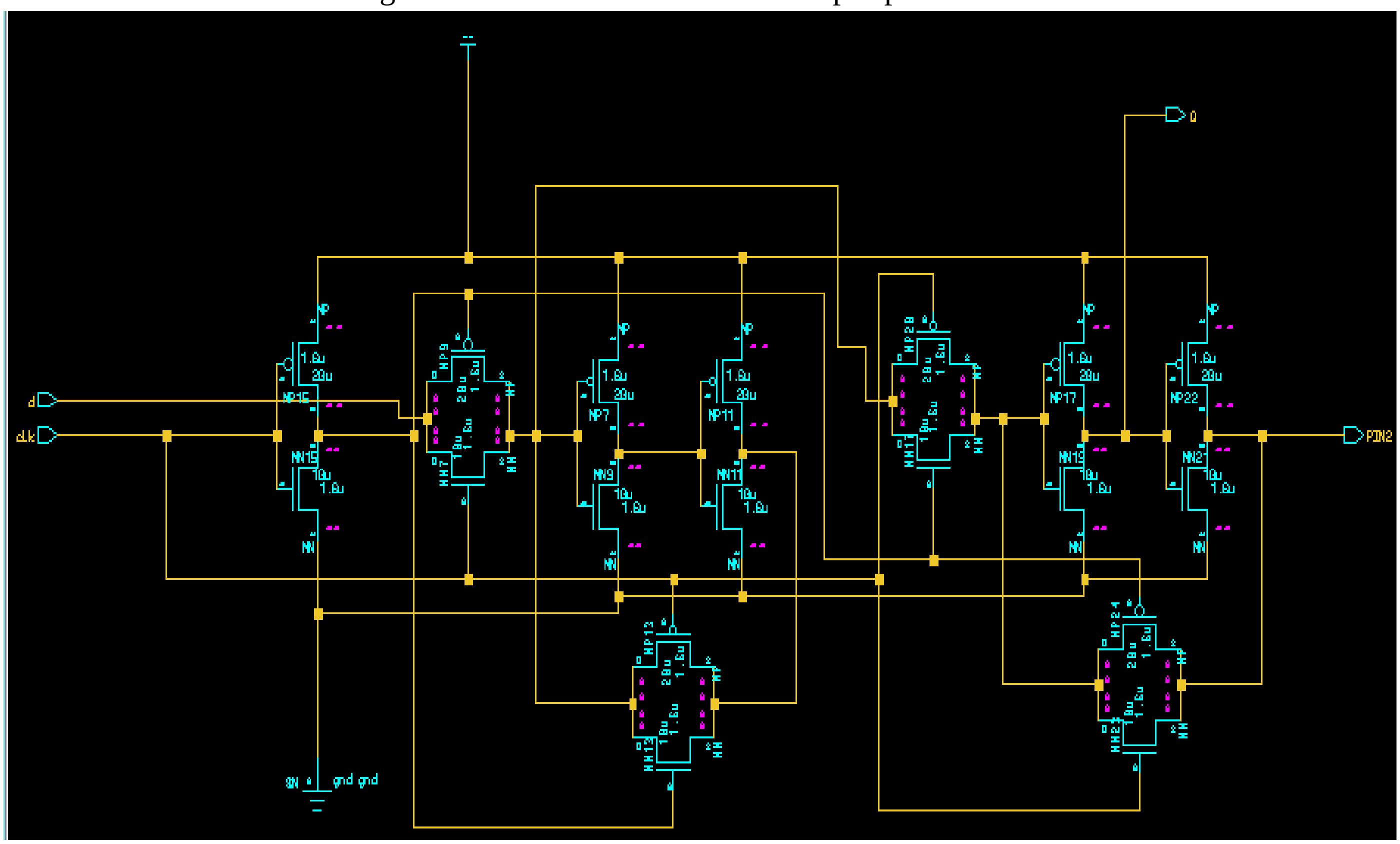


Figure 15: Schematic of D Flipflop

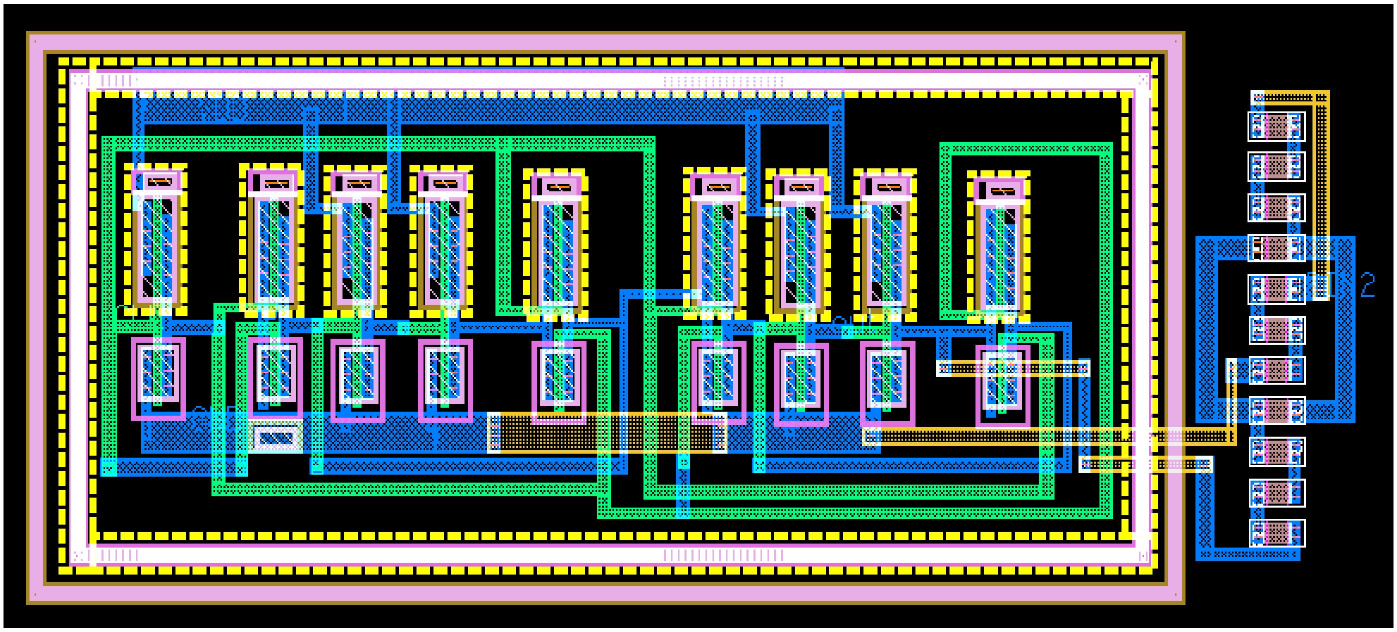


Figure 16: Layout of D Flipflop along with the resistor divider circuit (In the final layout for the complete system, the resistor-divider circuit is combined with the analog components and is isolated from the D Flipflop by means of guard rings)

Complete System

3.1 Whole system simulation

Till then, all the components were combined together, and the digital and analog parts of the circuit were separated from each other by using guard rings. The complete system simulation gave the desired result. System was initially tested for DC input voltages, and the final test was conducted using a sine wave. The simulation results for sine wave are shown below. The complete sine wave is shown first, followed by zoomed in sections of this same sine wave. The last simulation waveform shows the output of each stage in the complete system simulation, starting with the inputs and output of summer, followed by integrator output, comparator output and D Flip-flop output, which is the same as the system output.

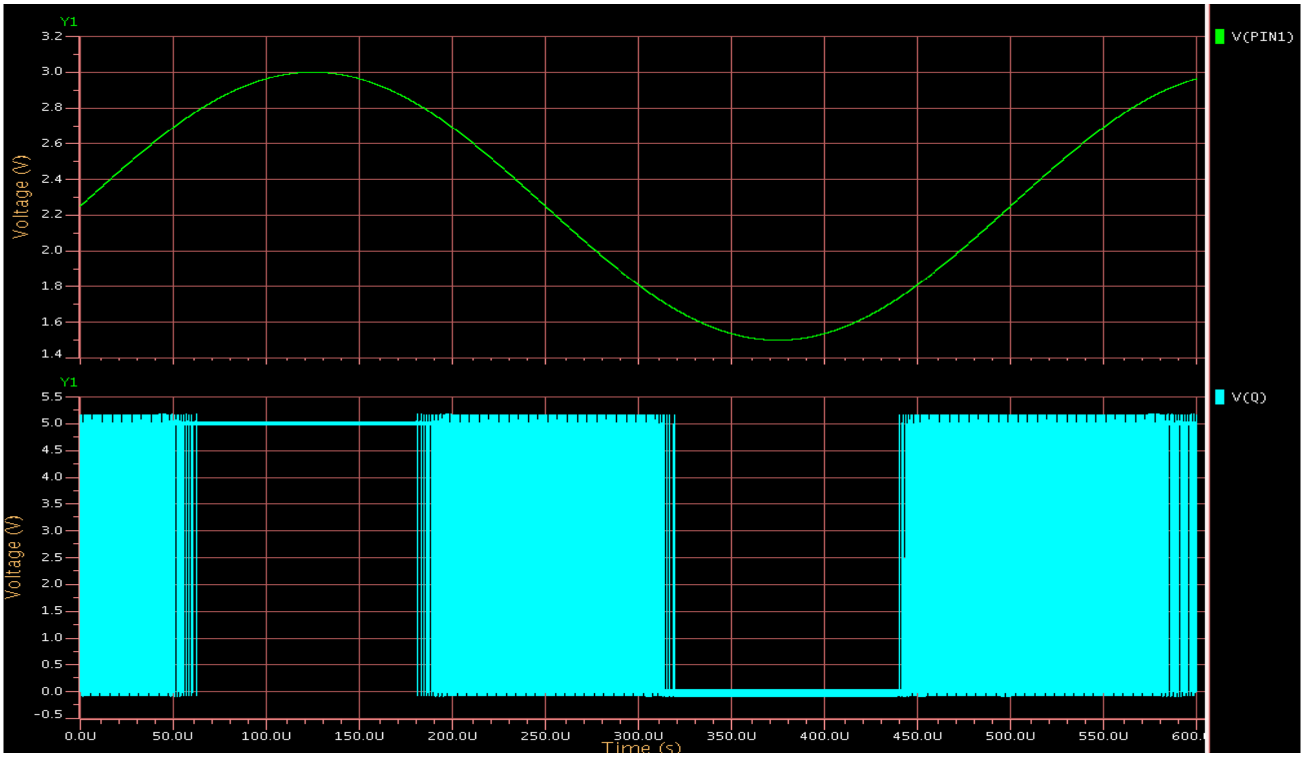


Figure 17: Output of the system for an analog sine wave input

There are more 1's near the top of the sine wave, and more 0's near the bottom of the sine wave. The first half of the sine wave above threshold has been zoomed in and shown in Figure 14.

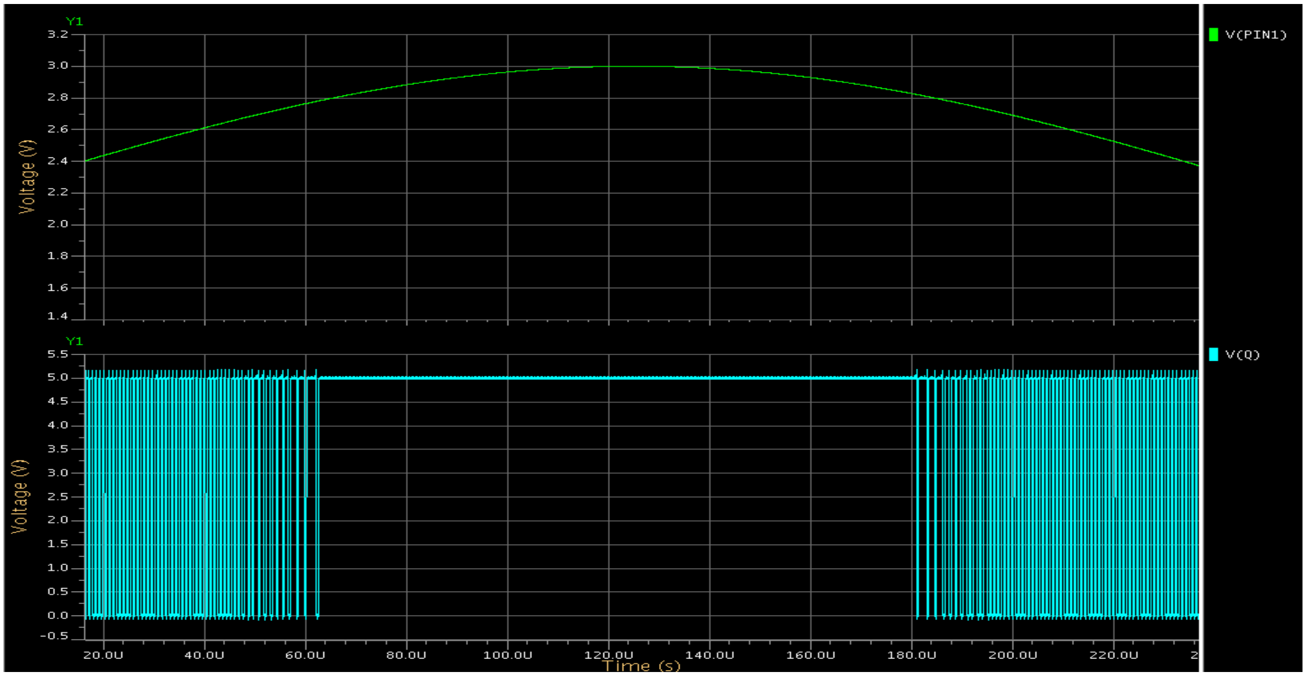


Figure 19: Portion of the sine wave above threshold

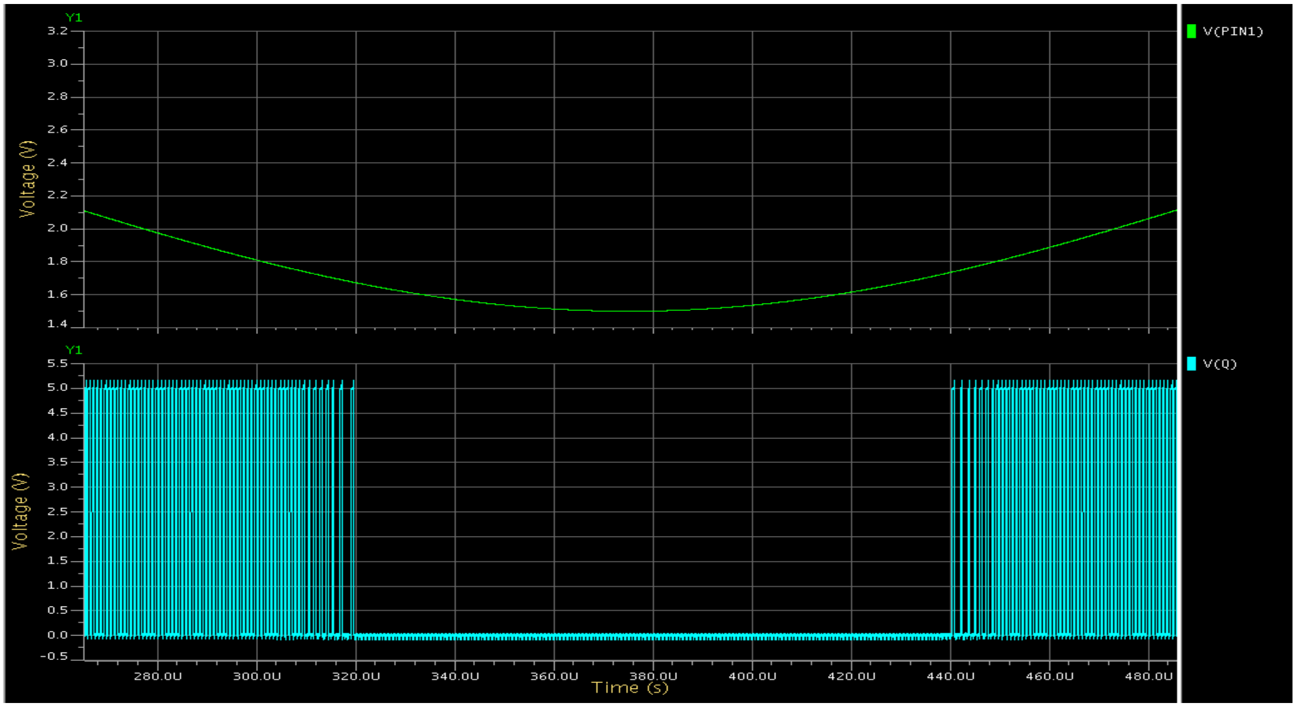


Figure 20: Portion of the sine wave below threshold

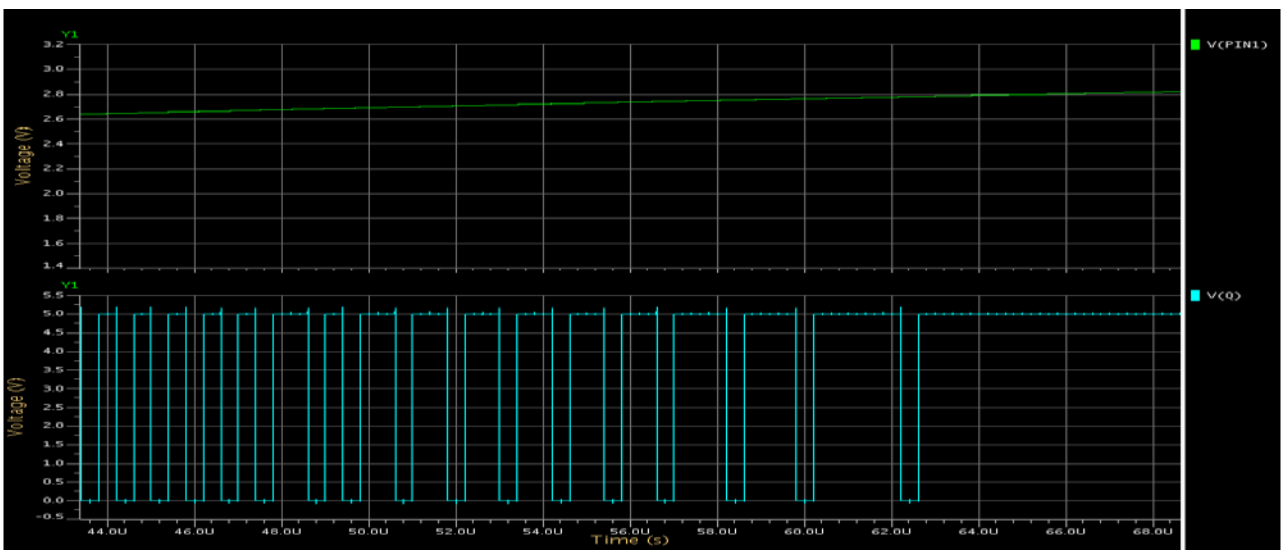


Figure 21: Increasing portion of sine wave **above threshold**. Since this is above threshold, therefore there are **more 1's** than 0's

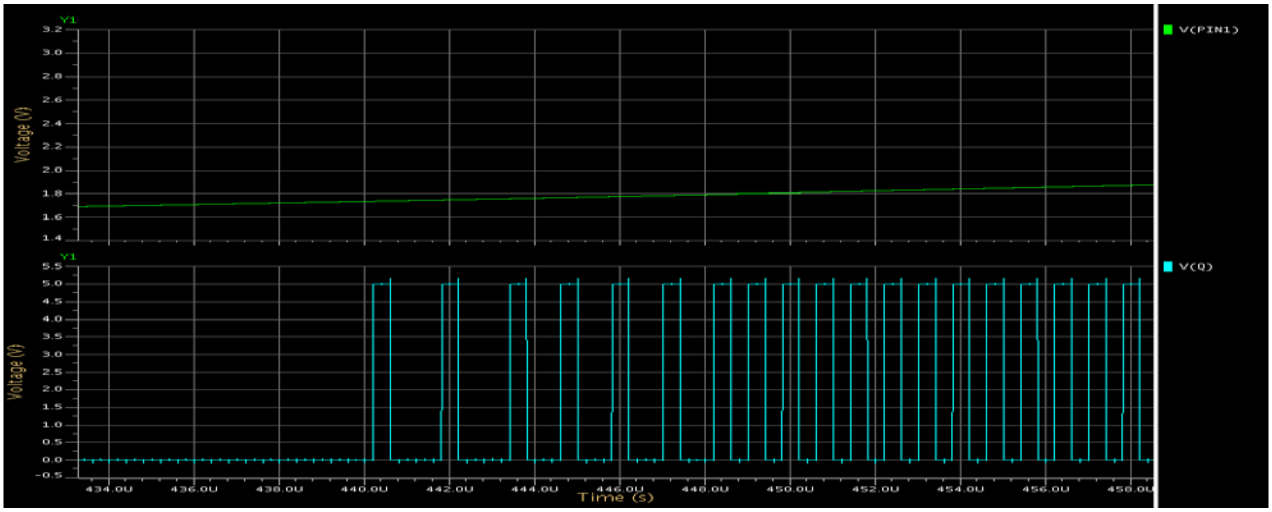


Figure 22: Increasing portion of sine wave **below threshold**. Since this is above threshold, therefore there are **more 0's** than 1's

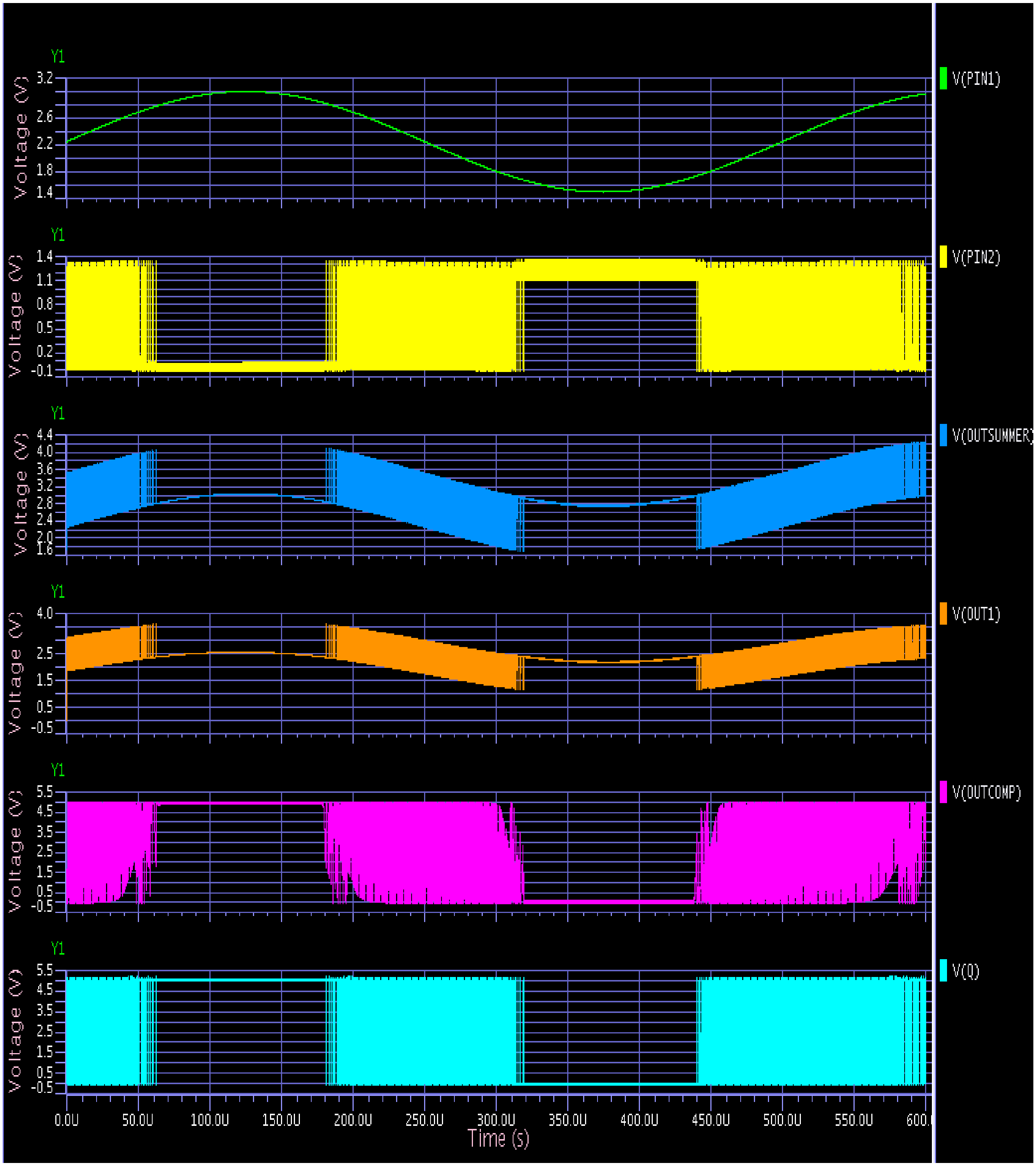


Figure 23: PIN1-Analog input to Summer, PIN2-output of modulator that is fed back to Summer through a resistor-divider circuit, OUTSUMMER- output of Summer, OUT1- output of integrator, OUTCOMP- output of Comparator, Q- output of D-Flipflop which is also the system output

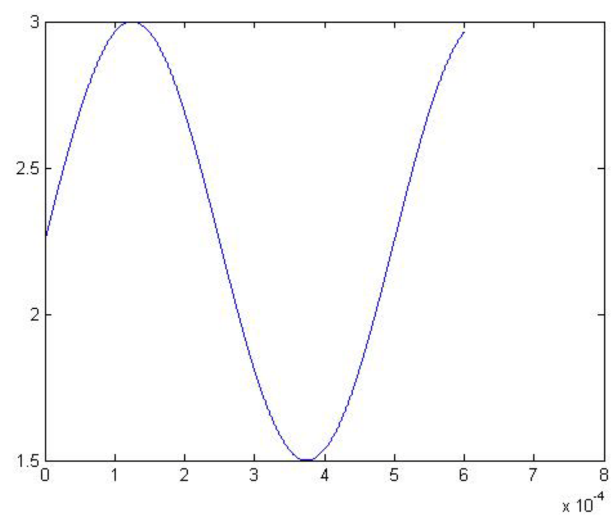
3.2 Whole system output analysis

Since the output of sigma-delta modulator is either 0 or 1, which are used to represent an analog signal. Thus, it is not easy to identify whether or not the system can convert signal into digital format correctly. So, we use some method to return pwm signal back to analog signal.

I used signal output generated from system hspice net list simulation and input the signal in Matlab through hspice toolbox. Writing m-file adding several voltages and get average value, I can draw a plot based on those average values. Bottom left one is the signal input into sigma delta modulates, the bottom right one is the transformed output based on 0 and 1. Basically, we can see output signal follows input signal, but there is some clipping and the waveform is not smooth at all.

Quantitative analysis:

Total point from output have 180,000 points, I pick average point every 500 points. Thus I have 360 points at all, making the graph below. Accordingly, our sigma delta modulator is around 8 bits (2^8=256).



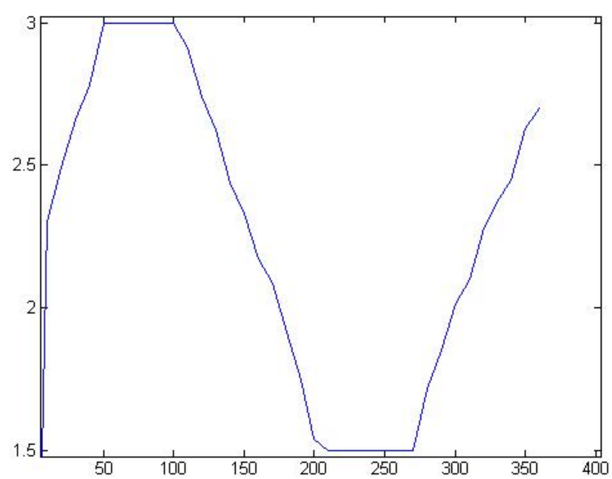


Fig 25 System input signal

Fig 26 System output transformed signal

3.3 System schematic and Layout

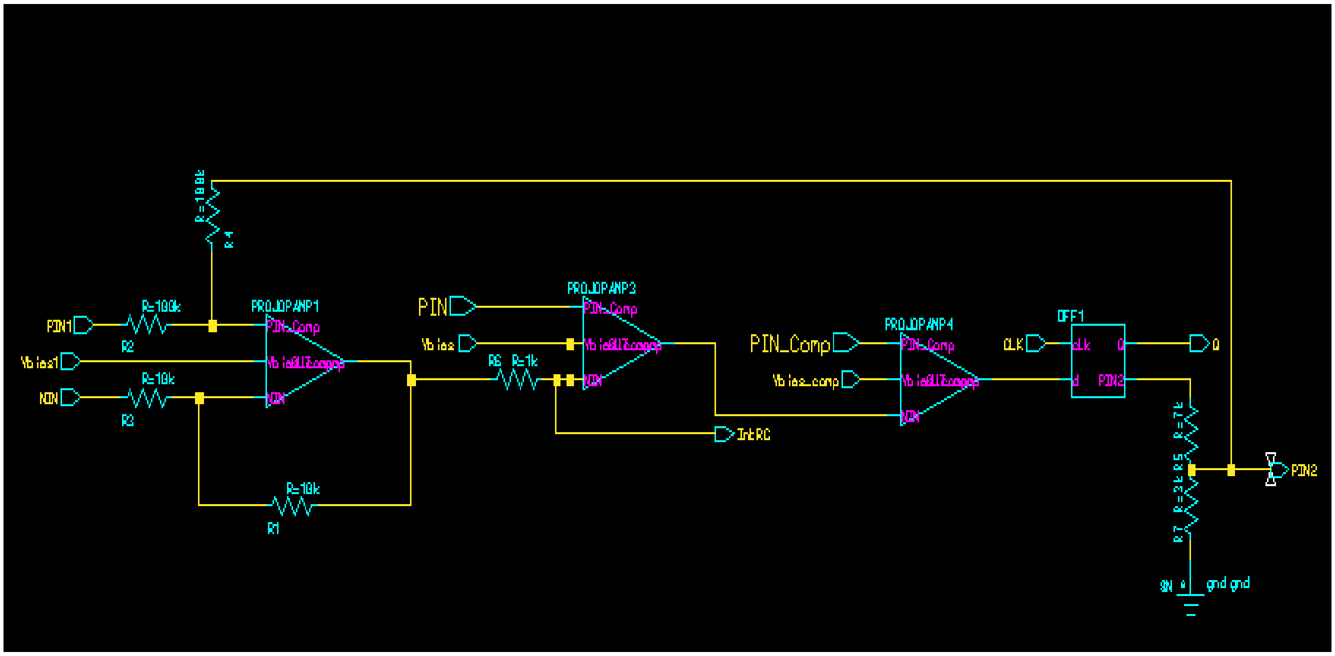


Figure 27: Schematic of complete system (Integrating capacitor is off-chip and is to be connected between IntRC and Output of integrator)

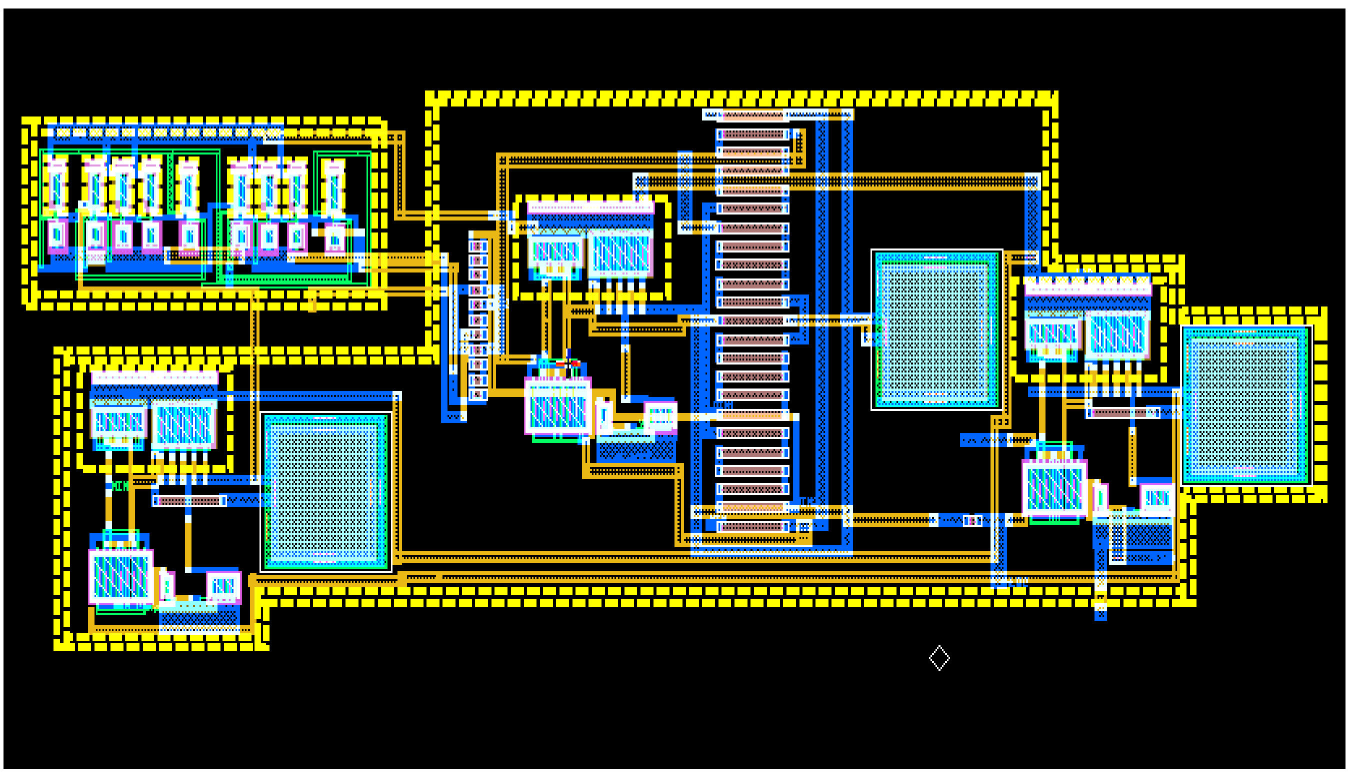


Figure 28: Layout of complete System

The complete system was DRC and LVS clean. Shown below is a screenshot which shows that the system is LVS clean.

```
REPORT FILE NAME:         /home/photinia/homes/fy11/mentor/lvs.rep
LAYOUT NAME:              $FY11LAY/SIG_DEL_GUARD
SOURCE NAME:              $FY11NETS/SYS/viewictrace
RULE FILE:                /opt/digital/share/mgc_hep/technology/ic/ami.5um.rules.3term
LVS MODE:                 Mask
RULE FILE NAME:           /opt/digital/share/mgc_hep/technology/ic/ami.5um.rules.3term
CREATION TIME:            Fri May  7 16:28:53 2010
CURRENT DIRECTORY:        /home/photinia/homes/fy11/mentor
USER NAME:                fy11

*****************************************************************************************
                               OVERALL COMPARISON RESULTS
*****************************************************************************************


                         #       ###################       _   _
                        #        #                 #       *   *
                   #   #         #     CORRECT     #         |
                    # #          #                 #       \___/
                     #           ###################
```

Figure 29: System is LVS clean

Conclusion

From the simulation and numerical analysis, we conclude that this sigma delta A/D converter can work in a proper condition and implement basic function as a converter. This device also inherits the merits of sigma delta A/D converter: high resolution but large area and low response time.

In design of this converter, our input range is from 1.5 – 3v while normal sigma delta ad converter has a positive-negative large input range and center their working voltage range at 0v, which leads to little or no off-set, while in our design center of working range is positive 3v, which leads to a certain off-set as well as some clipping during sampling.

The quantitative analysis is based on hspice simulation rather than layout extract netlist, since we have two off-chip components, a large capacitance and resistance. If we take them into account and wire capacitance and those parasite effects, it will be more difficult to expect the real output of our sigma delta converter. Besides, we did well in layout that we separate digital part (dff) and the rest analog part by surrounding and isolating, i.e. providing guard ring between them. Some parts of our circuit are common-centroided, thus effectively avoiding process variation locally.

Reference

[1] B. Razavi , *Design of analog CMOS integrated circuits:* Boston : McGraw-Hill, c2001.
[2] Hein, Søren, *Sigma Delta modulator: nonlinear decoding algorithms and stability analysis:* Boston : Kluwer Academic Publishers, c1993.

Appendix

1. M- file summing output

```
h=500;
i=180000/h;
ret=[0];
timeret=[0];
for j=1:i
    temp = 0;
    for n=1:h
        m=(j-1)*h+n;
        now = q(m,1);
        temp = now+temp;
    end
    ret= [ret;temp/h*1.5/5+1.5];
    timeret= [timeret;j];
end
```