

Green Hills Debug Probes Release Notes



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PubID: probe_release_notes-728395

Branch: <http://toolsvc/branches/probe-branch-6.6>

Date: November 18, 2022

Contents

Preface	xv
Host System Requirements	xvi
1. Version 6.6 Release Notes	1
New Features	2
New Supported Targets	2
New Trace Support	2
Additional New Project Wizard Support	3
New Chipset Support for Green Hills Probe v4 pterminal Command	3
Backwards Trace now supported on ETMv3	3
New ADIV6 Support	3
New locate Command	3
Support for 40-bit physical addresses on Cortex-A7 and Cortex-A15	4
Synchronous Run Control now supported on POWER e200	4
Changes in Behavior	4
"Show Target String" menu item in Green Hills Probe v4 LCD menu has been renamed to "Show Target Setting"	4
Xilinx ZYNQ-7000 Stand-alone BSP updated to use newer configuration convention	4
Removed Features	5
2. Version 6.4 Release Notes	7
New Features	8
Expanded Probe Support	8
New Supported Targets	8
New Trace Support	9
Additional New Project Wizard Support	9
New Flash Programmer Support	10
Improved Support for x86 and x64	10

New ADIV6 Support	10
GNJ Network Protocol on Green Hills Probe v4	10
Changes in Behavior	11
Probe CD Now Available in 32- and 64-bit Versions	11
PowerPC 4xx Trace Not Supported	11
Deprecated Features	11
Removed Features	11
3. Version 6.2 Release Notes	13
New Features	14
New Supported Targets for Green Hills Probe v4	14
New Trace Support	14
Additional New Project Wizard Support	15
Serial Port Forwarding on Green Hills Probe v4	15
Auto Detection of Trace Configuration and Diagnostics	15
Changes in Behavior	16
Cortex-R4 and Cortex-A8 Single-Core Trace	16
TLB vtag Format Changed on PowerPC QorIQ e6500 Targets	16
Deprecated Features	16
Removed Features	16
4. Version 6.0 Release Notes	19
New Features	20
Green Hills Probe v4	20
New Trace Support	21
USB Support for Linux	21
New Supported Targets	21
Additional New Project Wizard Support	21
New Command to Configure Coresight Paths	21
5. Version 5.6 Release Notes	23
New Features	24
New Supported Targets	24
Additional New Project Wizard Support	24

Changes in Behavior	25
New Installation Requirements	25
Removed Features	25
6. Version 5.4 Release Notes	27
New Features	28
New Supported Targets	28
Additional New Project Wizard Support	28
Support for ARM Embedded Trace Router and Embedded Trace FIFO Added	29
Support for ST SPC58NE84 Cut 1 and Cut 2	29
Changes in Behavior	29
Future Probe Software Will Require More Recent MULTI and Compiler Versions	29
Changes in Probe Treatment of WAIT Responses for CoreSight Targets	30
Both Embedded Trace Buffers Now Enabled on Vybrid	31
Changes to SuperTrace Probe trace_clock_delay Timing	31
Selecting "Retrieve When Buffer Fills" Causes Trigger on ARM ETB/ETR/ETF	31
Probe Cannot Update Directly from Pre-4.4 Firmware	31
Removed Features	31
Data Only Trace Option	31
7. Version 5.2.2 Release Notes	33
New Features	34
New Supported Targets	34
Additional New Project Wizard Support	34
New Trace Support	34
New Flash Support	34
New Support for Synchronous Multi-Core Systems	35
New Feature Support for Cortex-A15	35
TMC-ETB Support Added	35
Support for Heterogeneous Multi-Core CoreSight Systems	35
Probe Configuration Files Automatically Added to Projects and Loaded at Connection to MULTI	36

IEEE 1149.7 cJTAG Support for Freescale Targets	36
Support Added for MPC5744P Cut 2	36
Improved Support for Freescale Vybrid	37
New Probe Configuration Options	37
Changes in Behavior	37
use_swd Configuration Option Removed	37
New Syntax for Specifying CoreSight Targets	37
detect Command Changes	38
Big Endian Cortex-M Targets Now Supported	38
Removed Features	38
MPC5746M and MPC5777M e200z0 Core No Longer Available	38

8. Version 5.0.8 Release Notes 39

New Features	40
New Supported Targets	40
Additional New Project Wizard Support	41
New Trace Support	42
New Support for Target Trace Buffers	43
AXI-AP Support Added	43
New TraceEverywhere Parallel Trace Interface	43
Support Through the High-Speed Serial Trace (HSST) Aurora Interface	43
Probe Run Mode Support	44
Faster Power Architecture Trace Decoders	44
New Options for Fujitsu FCR4 Processors	44
Programming Spansion SPI Flash Memory Chips from Renesas RZ/A1	44
Changes in Behavior	44
Changed Use of trace_clock_phase Value	44
Changed Default of disable_swt Setting	45
Changes to Trace List Options	45
Defaults For jrst_ and rst_ Commands Changed	45
New Probe Configuration Files	46
MULTI 4 No Longer Supported	46

9. Version 4.4.4 Release Notes	47
New Features	48
New Supported Targets	48
Additional New Project Wizard Support	48
Support for Reading and Writing MPU Region Descriptors on Freescale MPC57xx	49
Support for Cortex-M4F VFP	49
Parallel Trace Decoding for ETMv3 Targets	49
10. Version 4.2.2 Release Notes	51
New Features	52
SWD Debug Interface Support	52
SuperTrace Probe v3 Debug and Trace Support for Additional Interfaces	52
BE8 Support for ARM11 and Cortex-R4	52
New Supported Targets for v3 Probes	52
Serial Port Forwarding Now Available	54
Removed Features	54
Diagnostics Pane of Probe Administrator is Not Available in MULTI 6	54
New Online Probe Manuals No Longer Available for MULTI 4.x on Linux	54
11. Version 4.0.2 Release Notes	55
New Features	56
New Supported Targets for v3 Probes	56
SuperTrace Probe v3	56
selftest Command	57
Changes to Existing Features	57
Changes to Timestamps	57
SuperTrace Probe v3 Does Not Have GPIO Pins	57
12. Version 3.8.2 Release Notes	59
New Features	60
Additional PowerPC Support	60

TraceEverywhere Cabling System	61
Changes and Fixes to Existing Features	61
Updated USB Driver	61
Probe Now Polls for Adapter and Power Status	61
Deprecated and Removed Features	62
IDT32 Processors Are No Longer Supported	62
13. Version 3.6.4 Release Notes	63
New Features	64
New ARM Features	64
Changes and Fixes to Existing Features	66
General Changed Features	66
14. Version 3.4.1 Release Notes	67
New Features	68
General New Features	68
New ColdFire Features	69
New PowerPC Features	70
Changes and Fixes to Existing Features	71
General Changed Features	71
ColdFire Changed Features	71
MIPS Changed Features	72
PowerPC Changed Features	73
15. Known Issues and Limitations	75
General Known Issues	76
Cache Visibility Features Show No Data in MULTI	76
Cannot Downgrade Firmware On Some Probes	76
Installation Disables ecomarm2 License	76
USB Driver Installation Fails on Windows Vista	76
Green Hills Probe v4 Requires mpadmin Included with Probe 6.0 CD or Later	77
General Issues Updating Probe Firmware	77
Probe Cannot Update Directly from Pre-4.4 Firmware	77
Connecting to Multiple USB Probes via the Probe Administrator	78

Green Hills Probe v4 USB Connections to Virtual Machines	78
Green Hills Probe v4 Does Not Support Simultaneous pterminal Connections	78
USB-Serial Device Disconnections May Be Silent	78
Unresponsive or Unreliable Network Connection	78
Errant Output from pterminal Session	79
Delayed pterminal Characters	79
Issues Interleaving MULTI Script and mperv Commands	79
Probe Administration Prompt Pane May Desynchronize After detect Command	80
Some Tabs Are Empty in the Register View Window	80
target tc and target th Behavior Changes when Halt Cores Synchronously is Selected	80
Incorrect Trace Decoding	81
Errors While Changing Trace Options on Multi-Core Targets	81
Changing Trace Options While Tracing May Result in Incorrect Trace Decoding on MULTI 7 and Earlier	81
Break on Trigger Only Halts Target If Target is Not Already Halted	81
Setting Options in the Trace Options Window Has No Effect When Data Trace is Disabled	82
Gap Between Timestamps in the Trace List or Path Analyzer	82
Trace Data Lost when Trace is Disabled Immediately After Retrieval	82
AddressSpaces Not Traced by Default After Disabling Trace	82
TimeMachine Demo Requires Specific Trace Options	82
Modifying Target State While Tracing May Cause Incorrect Memory or Register Reconstruction	83
Tracing a Program Running from ROM with a Setup Script	83
Target's Cores May Have Desynchronized Trace Timestamps	83
Timestamps May Overflow After 213 Days of Uptime	83
Trace Clear May Disable Trace Collection on MULTI 6	84
Entering and Leaving Debug Mode May Interfere with a Trace Disabled Packet	84
TE Pod logic_high Setting	84
Enabling Outputs Does Not Report an Error with Incorrect TE Adapter Setting	85

ARM Known Issues	85
Cannot View I-Cache or L2 Cache on Cortex-A5 Targets	85
Cannot Debug Certain Cache Configurations on Cortex-A5 and Cortex-A9 Targets	85
Issues Debugging the M4F Cores on i.MX8 QM and QXP While Caches are Enabled	86
Many TMS570 and R4x Processors Incorrectly Detected as a Cortex-R4F	86
No Access to XScale Cache Operations Register	86
bl Displays Duplicate Breakpoints	86
Slow Halt On ARM920 Target	87
Trigger Immediately Causes Two Triggers on CoreSight ETM11 Target	87
Triggers During Overflow May Be Dropped	87
Cannot Collect Trace Data on a Trigger on OMAP3	87
Freescale i.MX51 Does Not Work at Slow Clock Speeds	87
Some ETMv4 Features Are Not Supported	87
ETMv4 Triggers That Combine Execute Comparators with Data Access Comparators Are Not Reliable	88
Probe etm_register Options Must Be Manually Set on Multi-Core ETMv3 Targets	88
Trace Count for Accesses to or Execution of a Single Address on ETM Targets	88
Trace May Not Decode Correctly While Booting Cortex-A INTEGRITY Systems	89
Missed Trace Triggers in INTEGRITY Virtual AddressSpaces	89
Some ARM Cores Must Be Halted When Enabling Trace	89
ARM ETMv1 and ETMv3 64-Bit Data Accesses Displayed as 32-Bit Accesses in Trace List	90
Insufficient Trace Bandwidth for R-Car Evaluation Boards	90
Probe Cannot Detect Some ICEPick Targets	91
Some Data Missing from Trace Buffer on Cortex-M3 Targets	91
Some ARM11 CPUs Cause Incorrect Trace Data	91
Break on Trigger Does Not Trace Final Instruction on Cortex-R4	91
Enabling Trace on Multiple Running Cores	91
ARM Multi-Core Trace Targets with MULTI 6.x and Earlier May Require Enabling Trace Manually	92

Tracing ARM Targets Triggering Close to the Beginning of the Trace Buffer	92
Function and Callee's Filter Issue	93
SWD May be Unreliable on Freescale Vybrid	93
Flash Programming May Be Unreliable on Renesas RZ/A1 Board	93
Data Trace of Load/Store Multiple Instructions on ARM Targets with ETMv3.x with Incomplete Data	93
AArch32 Debug Not Supported	94
Issues Upgrading to Firmware 5.2	94
ARMv7 Trace	94
Trace May Not Reconstruct Canceling Exceptions on ETM Targets	95
Trace to the ETB with Triggers is Limited on the Vybrid	95
On ARM11, Instruction-Executed Trace Triggers May Trigger While Halted	95
ETMv3 Parallel Trace Decoding Limitation	95
Legacy ARM-20 Adapter Ignores Vref	95
ColdFire Known Issues	96
Power Detection Limitations	96
Breakpoint Limitations	96
Detecting a ColdFire Target with SuperTrace Probe	96
Problems Capturing Triggers on ColdFire V4 Targets	96
Undefined Behavior When Using the jp Command and the ColdFire Active Pod for GHP3	97
MIPS Known Issues	97
freeze_timers Disables the EN Bit in CTC1, CTC2, and CTC3	97
Low Level JTAG Procedures May Disrupt M4K Processors	97
Stepping Off of Breakpoints May Not Work When Debugging a Virtual Task	98
Accessible Physical Address Range Limited to 512 MB	98
TC Restrictions on MIPS 34K and 1004K Processors	98
Halt Cores Synchronously Not Supported with Multiple Subsets of Cores on MIPS	98
Power Architecture Known Issues	99
Incorrect Trace Decoding on PPC405 Processors	99
MPC5744P Stalls with Certain Trace Settings	99
Incorrect Trace with PowerPC e200 and MULTI 6	99

Censorship Unlock Requires Two Resets on PPC560x Processors	100
Little Endian Mode Is Not Supported on PowerPC e500-, e500mc-, e5500-, or e6500-based Targets	100
Incorrect PC Location After Halting Target	100
Locked Data Cache Not Supported on PowerPC 4xx Targets	100
Corrupted Registers When Setting an Execute Hardware Breakpoint on Some PowerPC Cores	100
Register Definitions Require Setting MULTI Variables	101
External Trace Trigger In Not Supported on PowerPC 405 Targets	101
Modifying Trigger Settings on PowerPC 4xx Targets	101
MPC564xC z0 Core Does Not Emit Trace Data on Single Step ...	101
Nexus Trace Does Not Support Read- or Write-Only Triggers	102
Nexus e200 MDO Width Limitations	102
MPC55xx and MPC56xx Trace Only Supports One Core at a Time	102
Single Stepping Over mtspr dbsrwr, rn May Not Execute As Expected on QorIQ P4040 and P4080	102
Triggers Are Not Supported on the e200z0 Core of the MPC564xC	103
Unexpected Machine Check On 567xR and 567xF	103
Trace Limitations with Stalling Enabled on MPC5777M e200z7 Cores	103
Incorrect Trace Decoding on MPC5748G Processors	103
Incorrect Trace Decoding on MPC5777M Processors	103
Incorrect Trace Decoding on MPC577xK Processors	104
Example T4240QDS Setup Script Should Not Be Canceled	104
Multi-Core Debug Limitations on QorIQ P3041	104
Trace Errata on Certain P4080/P4040 Silicon Revisions	104
Incorrect Trace Data on NXP QorIQ Processors with e500mc and e5500 Cores	104
Trigger Immediately Fails to Trigger After Retrieval	105
MPC5668 Stalls with Certain Trace Settings	105
Trace Limitations and Stalling on MPC574xB/C/G	105
Stalling on MPC5748G z210 Cores	105
Debugging SMP Applications Without OSA	106
Incorrect HSST Trace with Overflows on 57xx and 58xx	106

x86 Known Issues	106
Execute Hardware Breakpoints Cannot Exceed One Byte	106
x86 TraceEverywhere Adapters Not Supported with TraceEverywhere Trace Pod	106
Probe Cannot Configure Memory Mapping	106
tr Command Does Not Work as Expected on Some x86 Targets ..	107
MULTI Reports Any x86 Processor as a Pentium Pro	107
Cannot Write to Segment or Table Registers	107
Simultaneous Run-Mode and Freeze-Mode INTEGRITY Debugging Is Not Supported	107
Halt and Breakpoints on Sandy Bridge Targets Is Synchronous ...	107
Running Programs that Change Address Mappings	108
Software Breakpoints in SMP Debugging	108
Bootting a Multi-Core Target After Reset	108
Bootting a Multi-Core OS Clears Hardware Breakpoints on Secondary Cores	109
Target Halts in System Management Mode Code	109
Nehalem-Based Target Cannot Leave System Management Mode	109

Preface

Contents

Host System Requirements	xvi
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Thank you for choosing a Green Hills debug probe. These release notes cover what is new in this probe firmware release, what has changed, and other release-specific information that is not available in the standard documentation.

For installation information and instructions that explain how to configure your probe for your target, see the *Getting Started* book for your probe.

For reference information, see the *Green Hills Debug Probes User's Guide*.

Host System Requirements

Green Hills debug probe software runs on Windows and Linux. The current probe release requires 64-bit Compiler 2017.5 or later, as well as MULTI 7 or later and 300 MB of disk space. If you attempt to upgrade an older version of the tools, or a 32-bit version, the installer will give you an error. If you need to debug with 32-bit tools, use Probe version 6.4.



Note

If you have a v3 probe and need to debug a legacy target that is not supported with firmware 6.4 or later, use the 5.6 firmware located in *install_dir/ghprobe*.

Chapter 1

Version 6.6 Release Notes

Contents

New Features	2
Changes in Behavior	4
Removed Features	5

This section covers changes to the Green Hills Probe firmware that were added for version 6.6.

New Features

New Supported Targets

Firmware 6.6 adds run control for a number of new targets. For a complete list of supported targets, see the “Supported Devices” in Appendix E, “Supported Devices and Adapter Types” in *Green Hills Debug Probes User's Guide*.

All Probes

- NXP S32R264 (uses `ppcS32R274` target setting)
- NXP S32R274 (`ppcS32R274`)
- NXP S32R294 (`ppcS32R294`)
- NXP S32R372 (`ppcS32R372`)
- ST Micro SPC58xN series (`spc58NN`)
- Intel Tiger Lake (`tigerlake`)

Expanded Green Hills Probe v4 Support

All ColdFire targets previously supported on v3 probes are now also supported on GHPv4 for run control and trace.

New Trace Support

Trace support is now available for the following:

- Cortex-M33
- NXP S32R264
- NXP S32R274
- NXP S32R372

- ST Micro SPC58xN

Additional New Project Wizard Support

Now included:

- NXP S32R274 Demo Board (S32R274 CPU)
- NXP S32R274 Demo Board (S32R372 CPU)
- NXP S32R294 Demo Board
- ST Micro SPC58NN84 EVB

New Chipset Support for Green Hills Probe v4 pterminal Command

pterminal now supports USB-Serial devices using Silicon Labs CP210X chipsets connected to the front target USB port of the Green Hills Probe v4. For more information, see “Serial Port Forwarding” in Chapter 3, “Probe Connection Reference” in *Green Hills Debug Probes User's Guide*.

Backwards Trace now supported on ETMv3

Backwards Trace (requires MULTI 8) is now supported on all ETMv3 targets when collecting trace to Trace Probe memory. Backwards Trace decodes trace backwards from the most recently collected trace packets, allowing immediate TimeMachine debugging of the most recently executed code, while earlier trace data continues to be decoded. This feature is also supported on all ETMv4 targets.

New ADIv6 Support

ADIv6 is now supported for Cortex-M CPUs, and for non-CPU CoreSight devices. In addition, support for MEM-APs attached to other MEM-APs is added.

New locate Command

Firmware 6.6 adds the **locate** command for STPv3 and GHPv4. This can be used to help locate a probe by playing a sound and flashing its display. For more

information, see the **locate** command in “System Commands” in Chapter 5, “Probe Command Reference” in *Green Hills Debug Probes User's Guide*.

Support for 40-bit physical addresses on Cortex-A7 and Cortex-A15

The probe now supports 40-bit physical addresses on Cortex-A7 and Cortex-A15. For more information, see the **table_base** configuration option in “Target-Specific Configuration Options” in Chapter 4, “Probe Option Reference” in *Green Hills Debug Probes User's Guide*.

Synchronous Run Control now supported on POWER e200

The "Halt Cores Synchronously" feature in **mpserv** (and the associated **-synccores** argument) is now supported with multicore POWER e200 processors.

Changes in Behavior

"Show Target String" menu item in Green Hills Probe v4 LCD menu has been renamed to "Show Target Setting"

On newly fielded probes, the "Show Target String" LCD menu name has changed to "Show Target Setting." Documentation references have been updated accordingly. Previously fielded probes will still show "Show Target String" on the LCD screen.

Xilinx ZYNQ-7000 Stand-alone BSP updated to use newer configuration convention

The probe configuration files and setup script included with the Xilinx ZYNQ-7000 stand-alone BSP have been updated to use the `csdap` target setting syntax as well as CoreSight paths to configure trace. Note that these configuration files should be used together; mixing and matching a new setup script with an old probe configuration will not work (and vice versa).

Removed Features

The following features are no longer available:

- The probe installer no longer supports 32-bit tools.

Chapter 2

Version 6.4 Release Notes

Contents

New Features	8
Changes in Behavior	11
Deprecated Features	11
Removed Features	11

This section covers changes to the Green Hills Probe firmware that were added for version 6.4.

New Features

Expanded Probe Support

Firmware 6.4 is the first firmware release that is backwards compatible, supporting Green Hills Probe v4 and the previous generation v3 probe devices.

New Supported Targets

Firmware 6.4 adds run control for a number of new targets. For a complete list of supported targets, see the “Supported Devices” in Appendix E, “Supported Devices and Adapter Types” in *Green Hills Debug Probes User's Guide*.

All Probes

- Cortex-M23 (`csdap(m23)`).
- Cortex-M33 (`csdap(m33)`).
- Cortex-R52 (`csdap(r52)`).
- Cortex-R8 (`csdap(r8)`).
- Cortex-A55 (`csdap(a55)`).
- Cortex-A73 (`csdap(a73)`).
- Cortex-A76 (`csdap(a76)`).
- ST Micro SPC58NH series (`spc58NH`).
- Intel Atom Apollo Lake (`atom_gm`).
- RISC-V.



Note

RISC-V Debug Modules and JTAG Debug Transport Modules are supported if they are compatible with version 0.13.2 of the External Debug Support specification.

Expanded Green Hills Probe v4 Support

A number of legacy ARM and PowerPC targets are now supported on GHPv4. This includes targets from the PowerPC processor families G2, 7xx, 74xx, e300, e600, 440 and popular members of the ARM processor families ARM7, ARM9, and XScale.

Expanded v3 Probes Support

All targets listed as newly supported in firmware 6.0 and 6.2 are now supported on v3 probes.

New Trace Support

Trace support is now available for the following ARMv8-A SOCs (requires Compiler 2017.1 or newer):

- Cortex-R8.
- ST Micro SPC58NH series.
- Renesas R-Car M3W.
- Renesas R-Car D3.
- Renesas R-Car V3H.
- Renesas R-Car V3M.

Additionally, trace support is available for debugging INTEGRITY on the Renesas R-Car M3W, D3, V3H, and V3M (see “Tracing INTEGRITY on AArch64” in Appendix D, “Troubleshooting and Usage Notes” in *Green Hills Debug Probes User's Guide*).

Additional New Project Wizard Support

Now included:

- CYTVII-B-E-176-CPU with TVII-B-E-2M.
- ST Micro SPC58NH92 EVB.
- Renesas R-Car D3 Draak.

- Renesas R-Car V3H Condor.
- Renesas R-Car V3M Eagle.
- NXP i.MX RT 1050-EVKB.
- NXP KV58F220M Tower.
- Atmel SAM V71 Xplained Ultra.

New Flash Programmer Support

Probe host tools now support programming these devices:

- STM32H7 internal flash.
- SPI flash connected to STM32H7.
- SPI flash connected to FTSPi020 controller on ARM.
- S32K3 internal flash.

Improved Support for x86 and x64

Several improvements have been made to x86/x64 support:

- Debugging x64 is now supported. (Intel Atom Apollo Lake is considered x64 by default.) If you need to debug a 32-bit program, you can force your probe to use 32-bit mode by passing **-ia32** to **mpserv**.
- Accessing MSRs and I/O registers is now supported. For more information, see the x86 section of “Target-Specific Special Registers” in Chapter 5, “Probe Command Reference” in *Green Hills Debug Probes User's Guide*.

New ADIv6 Support

ADIv6 is now supported for ARMv8-A and ARMv8-R CPUs.

GNJ Network Protocol on Green Hills Probe v4

GNJ is a network protocol designed to replace the probe's physical interface when a physical connection to a target is not feasible. For more information, see

“Debugging with GNJ (GHPv4 Only)” in Chapter 3, “Probe Connection Reference” in *Green Hills Debug Probes User's Guide*.

Changes in Behavior

Probe CD Now Available in 32- and 64-bit Versions

The Probe CD is now available in both 32- and 64-bit versions. You must use a version of the toolchain with a corresponding bitness (32- or 64-bit).

PowerPC 4xx Trace Not Supported

Firmware 6.4 does not support trace on PPC4xx. Contact Green Hills support if you require PPC4xx trace support.

Deprecated Features

The following features are deprecated and will be removed in a future release:

- Firmware 6.4 is the last probe release that will support 32-bit toolchain versions. Firmware 6.6 and later will support only 64-bit toolchain versions.

Removed Features

The following features are no longer available:

- The Probe CD will no longer install firmware 4.4 or firmware 5.4 for older versions of the toolchain. MULTI 6 is no longer supported.

Chapter 3

Version 6.2 Release Notes

Contents

New Features	14
Changes in Behavior	16
Deprecated Features	16
Removed Features	16

This section covers changes to the Green Hills Probe firmware that were added for version 6.2.

New Features

New Supported Targets for Green Hills Probe v4

Firmware 6.2 adds run control for the following targets:

- Cortex-A35 (`csdap(a35)`).
- Cortex-A72 (`csdap(a72)`).
- Zynq UltraScale+ MPSoC (`mpsoc`).
- NXP QorIQ T1013 (`ppcT1013`).
- NXP QorIQ T1014 (`ppcT1014`).
- Qualcomm Kryo (`csdap(kryo)`).

Additionally, cores and processors that were previously supported on v3 probes from the following families are now supported on Green Hills Probe v4:

- Cortex-A (including trace support for ETMv3 and PTM).
- NXP PowerPC/QorIQ e500, e5500, and e6500 (no trace support at this time).

Note that firmware 6.2 is only supported on the Green Hills Probe v4. For a full list of supported targets, see “Supported Devices” in Appendix E, “Supported Devices and Adapter Types” in *Green Hills Debug Probes User's Guide*.

New Trace Support

Trace support is now available for the following ARMv8-A SOCs (requires Compiler 2016.5 or newer):

- NXP i.MX 8M.
- NXP i.MX 8X.
- Renesas R-Car H3.
- Zynq Ultrascale+ MPSoC.

Additionally, trace support is available for debugging INTEGRITY on the Renesas R-Car H3 Salvator-XS (see “Tracing INTEGRITY on AArch64” in Appendix D, “Troubleshooting and Usage Notes” in *Green Hills Debug Probes User's Guide*).

Additional New Project Wizard Support

Now included in Compiler 2018.5 or newer:

- NXP i.MX8 QM
- NXP i.MX8 QXP

Now included in Compiler 2015.1 or newer:

- Zynq UltraScale+ MPSoC.

Now included in Compiler 2014.1 or newer:

- Renesas R-Car Gen3 M3-W Salvator-XS.

Now included in Compiler 2013.5 or newer:

- NXP QorIQ LS1021A.

Serial Port Forwarding on Green Hills Probe v4

The **pterminal** command is now supported on Green Hills Probe v4 using the target USB port on the front of the probe. Only USB-Serial devices using the FTDI FT232R chipset or the Prolific chipset are supported at this time. For more information, see “Serial Port Forwarding” in Chapter 3, “Probe Connection Reference” in *Green Hills Debug Probes User's Guide*.

Auto Detection of Trace Configuration and Diagnostics

You can now use the **detect -trace** command to automatically set **trace_logic_high** and to calibrate the **trace_capture_offset** value. Using **detect -trace** will also perform basic trace pin diagnostics to identify non-toggling trace pins. For more information, see **detect** in Chapter 5, “Probe Command Reference” in *Green Hills Debug Probes User's Guide*.

Changes in Behavior

Cortex-R4 and Cortex-A8 Single-Core Trace

Tracing single-core Cortex-R4 or Cortex-A8 targets is now done in CoreSight continuous mode by default. Previous probe releases used bypass mode by default. To restore the old behavior, add `.bypass` to the core name in your target string. For example, if you used the target setting `cortexr4 other(4, 0xf)`, you should now use `cortexr4.bypass other(4, 0xf)`.

TLB vtag Format Changed on PowerPC QorIQ e6500 Targets

The probe's **tlbw** command has a *vtag* argument that can be entered as a hexadecimal or symbolic value. The mapping of the hexadecimal value's bits to TLB tags has changed (see Appendix C, “CPU-Specific Bit Tables” in *Green Hills Debug Probes User's Guide*). The **tlbr** command's output reflects this change.

Deprecated Features

The following features are deprecated and will be removed in a future release:

- Concurrent Debugger connections to the same probe are no longer supported. The **single_mpserv_only** configuration option, which controls this feature, is deprecated, and will be removed in a future firmware. The `on` setting for this option is the only supported setting and will be the default behavior in a future firmware. Contact Green Hills Support if you need multiple Debugger connections to the same probe simultaneously.

Removed Features

The following features are no longer available:

- The `imx51_t02` target setting. The Freescale iMX51 SoC is supported with the `csdap(a8)` target setting by setting **ignore_csypwrupack** to `off`.
- Support for the Freescale i.MX51 stand-alone BSP, as it is no longer distributed. If you require this BSP, please contact Green Hills Support.

- Support for MULTI 6.1.4. MULTI 6.1.6 and newer remain supported. We recommend that you use the latest version of MULTI.
- Support for the NXP S32V234-EVB stand-alone BSP, as it is no longer distributed. If you require this BSP, please contact Green Hills Support.

Chapter 4

Version 6.0 Release Notes

Contents

New Features	20
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This section covers changes to the Green Hills Probe firmware that were added for version 6.0.

New Features

Green Hills Probe v4

Firmware 6.0 adds support for Green Hills Probe v4, the next generation of Green Hills Software's JTAG debug probes. The probe's new capabilities include:

- Faster download speeds.
- Up to 4 GB of trace memory.
- Aggregate trace bandwidth of 4.8 GB per second.
- 12 Gb high-speed serial trace support.
- Target power control and monitoring.
- Target network switching.
- 5V JTAG support.

Firmware 6.0 only supports Green Hills Probe v4, and does not yet support all features previously released for Green Hills Probe v3 and SuperTrace Probe v3. Here are the notable differences:

- Firmware 6.0 includes support for all previously supported POWER e200 processors, ARM Cortex-M, and ARM Cortex-R cores. For a list of supported targets, see “Supported Devices” in Appendix E, “Supported Devices and Adapter Types” in *Green Hills Debug Probes User's Guide*.
- Firmware 6.0 supports serial and parallel trace connections to ARM processors, but only parallel trace connections to POWER processors.
- Firmware 6.0 does not support serial port forwarding. The **pterminal** command will support USB serial devices connected to the target USB port (on the front of the probe) in a future release.

New Trace Support

Trace support is now available for the following targets:

- Cortex-R7 and Cortex-M7 targets with ETMv4.
- ST Micro SPC570S50.
- NXP MPC5748G.
- NXP MPC5746C.

USB Support for Linux

USB connections to probes from **mpserv** and **mpadmin** are now supported for Linux. (USB support for **Probe Administrator** on Linux will be added in a future version of MULTI.)

New Supported Targets

Run control and trace support is now available for the following targets:

- ST Micro SPC574S60 (`spc574S60`).

Additional New Project Wizard Support

New Project Wizard support is now available for the following boards:

- ST Micro SPC574S60 EVB.

New Command to Configure Coresight Paths

A new command (**coresight_path**) allows you to configure paths between trace sources and trace sinks on Coresight targets. It is required for configuring ETMv4 targets, and also supported on ETMv3 and PTM targets. For more information, see the table in “Configuration Commands” in Chapter 5, “Probe Command Reference” in *Green Hills Debug Probes User's Guide*.

Chapter 5

Version 5.6 Release Notes

Contents

New Features	24
Changes in Behavior	25
Removed Features	25

This section covers changes to the Green Hills Probe firmware that were added for version 5.6.

New Features

New Supported Targets

The following targets are now supported:

- Cortex-M7 (`csdap(m7)`).
- Cortex-R7 (`csdap(r7)`).
- NXP MPC5746B (`ppc5746B`).
- NXP MPC5746C (`ppc5746C`).
- ST SPC58xx 2B-line.
 - ST SPC582B (`spc582B`).
- ST SPC58xx 4B-line.
 - ST SPC584B (`spc584B`).
- ST SPC58xx C-line.
 - ST SPC58EC (`spc58EC`).
 - ST SPC584C (`spc584C`).

Additional New Project Wizard Support

Now included in Compiler 2013.5 or newer:

- NXP (Freescale) MPC5746C Demo Board.
- ST SPC582Bxx EVB.
- ST SPC58EC EVB.
- ST SPC584B EVB.

Now included in Compiler 2014.1 or newer:

- Renesas R-Car H3 Salvator-X.

Now included in Compiler 2015.1 or newer:

- ST STM32F779I-EVAL.

Changes in Behavior

New Installation Requirements

MULTI 5 and Compiler versions prior to 2013.5 are no longer supported. If you install probe firmware and software support 5.6 over Compiler 2013.1 or earlier version 5.4.4 will be installed instead.

Removed Features

- The **dhcp_lease** option. All DHCP leases will not request a specific lease duration and will use whatever the server assigns.
- Solaris support.
- Tracing the Cortex-M4 core using the S32V234-EVB stand-alone BSP. If you require this functionality, please contact support.

Chapter 6

Version 5.4 Release Notes

Contents

New Features	28
Changes in Behavior	29
Removed Features	31

This section covers changes to the Green Hills Probe firmware that were added for version 5.4.

New Features

New Supported Targets

The following targets are now supported:

- Cortex-A7 (`csdap(a7)`).
- Cortex-A53 (`csdap(a53)`).
- Cortex-A57 (`csdap(a57)`).
- Generic ARMv8-A (`csdap(armv8a)`).
- NXP MAC57D5xx (`mac57d54h`).
- NXP MPC5777C (`ppc5777c`)
- NXP QorIQ T1020 (`ppcT1020`)
- NXP QorIQ T1040 (`ppcT1040`)
- NXP QorIQ T2080 (`ppcT2080`)
- ST SPC58NE84 (`spc58NE84`)

Additional New Project Wizard Support

Support for the following boards is now included in Compiler 2012.5 or newer:

- NXP MAC57D54H EVB.
- NXP MPC5777C Demo Board.
- Renesas R-Car H2 Lager.
- Renesas R-Car E2 Silk.
- Spansion Traveo, includes S6J311AH, S6J311EJA, and S6J326CL. The S6J326CL project also supports the S6J32BALS CPU.
- ST SPC58NE84 EVB

Support for the following boards is now included in Compiler 2013.1 or newer:

- NXP T1040DS.
- NXP T2080RDB.

Support for the following boards is now included in Compiler 2015.1 or newer:

- NXP S32V234-EVB.
- APM XGene X-C1 Evaluation Kit.

Support for ARM Embedded Trace Router and Embedded Trace FIFO Added

This release adds support for collecting trace to ARM's Embedded Trace Router and Embedded Trace FIFO. This feature allows targets containing an ETR or ETF to be traced with a Green Hills Probe or SuperTrace Probe. Embedded Trace FIFOs that are not used as trace sinks will be automatically configured to run in Hardware FIFO mode. For more information, see the Trace Sink option in “Target-Specific Trace Options” in Chapter 4, “Probe Option Reference” in *Green Hills Debug Probes User's Guide*.

Support for ST SPC58NE84 Cut 1 and Cut 2

The probe now supports the ST SPC58NE84 cut 1 and cut 2 silicon. The board's default configuration in New Project Wizard will work with both cuts, but will exclude 32K of available SRAM on cut 1. For more information or to adjust these settings, see *install_dir/target/ppc/spc58ne84/board_info.txt*.

Changes in Behavior

Future Probe Software Will Require More Recent MULTI and Compiler Versions

Probe firmware 5.4 is the last version that will support MULTI 5.x, Compiler 2012.1, Compiler 2012.5, and Compiler 2013.1. Future probe releases will require Compiler 2013.5 or later. To accommodate older compiler installations, post-5.4 versions of the probe CD will continue to include firmware 5.4. If Compiler 2013.1 or earlier

is specified as an installation directory, version 5.4 will be installed instead of the latest firmware.

Changes in Probe Treatment of WAIT Responses for CoreSight Targets

Certain low-level SWD and JTAG scans can return a WAIT response, meaning that the target was not ready for the scan and thus the scan will be retried. There have been several changes in probe treatment of WAIT responses:

- Prior to firmware 5.4, these low-level scans were subjected to a fixed timeout of 250ms for JTAG targets and 1000ms for SWD targets. If the target failed to provide a non-WAIT response within these periods, the scan would fail. In firmware 5.4, the timeout defaults to 50ms and is configurable. For more information, see **coresight_timeout** in the ARM configuration options in Chapter 4, “Probe Option Reference” in *Green Hills Debug Probes User's Guide*.
- Prior to firmware 5.4, receiving a reserved encoding from a JTAG DPACC or APACC ACK field triggered a WAIT response. In firmware 5.4, if a probe receives a reserved encoding from the target, it is treated as an error and the scan is not retried.

There are two primary consequences to these changes:

1. Some exceptionally slow targets—typically only emulated CPUs—will require the **coresight_timeout** option to be increased.
2. Some targets will provide invalid ACK responses to CoreSight scans shortly after reset is released. This issue can arise because invalid ACK responses used to result in a retry with a lengthy timeout, which would cause the probe to continue retrying until CoreSight scans began working. To avoid this issue, you may need to increase **rst_settle**, **jrst_settle**, and **power_on_settle**. For more information, see Chapter 4, “Probe Option Reference” in *Green Hills Debug Probes User's Guide*.

Additional complications may arise if your target provides an invalid ACK response when it should provide a WAIT response. Although Green Hills Software knows of no such targets, if you believe you have such a target, please contact Green Hills Support.

Both Embedded Trace Buffers Now Enabled on Vybrid

Firmware 5.4 now presents both Vybrid ETB cores to the trace tools. Use the **Trace Sink** option to select an ETB core. Options on the ETB cores are now read-only, which may cause old probe configuration files to fail to load. Updated probe configuration files are included in the 5.4 release.

Changes to SuperTrace Probe trace_clock_delay Timing

Due to stability and performance improvements, trace capture alignment on the TraceEverywhere pod has changed. If you recently upgraded to firmware 5.4, and if the **trace_clock_source** option on your probe is set to `p11`, you may experience incorrect trace decoding. To ensure optimal trace capture, you may need to re-calibrate your **trace_clock_delay** value.

Selecting "Retrieve When Buffer Fills" Causes Trigger on ARM ETB/ETR/ETF

For users of ARM ETB, ETR, or ETF trace sinks, selecting the **Retrieve When Buffer Fills** check box in the **Trace Options** window now sets an immediate trigger on the target. Note that this trigger will be present in the trace of each capture.

Additionally, setting a trigger in the **Trace Triggers** window and then selecting **Retrieve When Buffer Fills** will cause the specified trigger to not be used.

Probe Cannot Update Directly from Pre-4.4 Firmware

Probe firmware versions prior to 4.4 will not directly update to probe firmware version 5.4 or later. For more information, see “Probe Cannot Update Directly from Pre-4.4 Firmware” on page 77.

Removed Features

Data Only Trace Option

The Data Only Trace option is no longer available. Please contact Green Hills Support if you require access to this feature.

Chapter 7

Version 5.2.2 Release Notes

Contents

New Features	34
Changes in Behavior	37
Removed Features	38

This section covers changes to the Green Hills Probe firmware that were added for version 5.2.

New Features

New Supported Targets

Support for the following targets was added in version 5.2.2:

- Avago AXX55xx (axx5500)
- Freescale MPC577xK (ppc5775K)
- Freescale QorIQ T4160 (ppcT4160)
- Freescale QorIQ T4240 (ppcT4240)

Additional New Project Wizard Support

New Project Wizard support for the following boards was added in version 5.2.2:

- Freescale MPC5775K Demo Board
- Freescale T4240DS

Support for these boards will be installed into Compiler 2012.5 or newer.

New Trace Support

The SuperTrace Probe v3 now supports debugging and tracing the following targets:

- Freescale Qorivva 57xx targets, over the high-speed serial trace (HSST) Aurora interface.

New Flash Support

The following flash chips are now supported:

- MPC57xx and SPC57x processors – for more information, see “Programming the UTest Block” in Appendix D, “Troubleshooting and Usage Notes” in *Green Hills Debug Probes User's Guide*.

New Support for Synchronous Multi-Core Systems

The probe now supports locking cores in a multi-core system, so that all cores in the system always resume and halt at the same time. This feature also enables software breakpoints to be set on all cores at the same time. For more information, see **Halt cores synchronously** in “Green Hills Debug Probe (mpserv) Advanced Settings” in Chapter 3, “Probe Connection Reference” in *Green Hills Debug Probes User's Guide*. This feature is only supported on ARM Cortex-A and POWER e500mc, e5500, and e6500 targets at this time, and requires MULTI 7 or later.

New Feature Support for Cortex-A15

The following features are now supported on the Cortex-A15:

- L1 and L2 cache visualization
- TLB visualization
- Trace Support

TMC-ETB Support Added

This release adds support for ARM's Trace Memory Controller when configured as an Embedded Trace Buffer (TMC-ETB). This feature allows targets containing a TMC-ETB to be traced with a Green Hills Probe as well as a SuperTrace Probe.

Support for Heterogeneous Multi-Core CoreSight Systems

The Green Hills Probe now supports debugging systems that contain multiple CPU cores of different types behind a single CoreSight DAP. See “Specifying CoreSight Targets” in Chapter 4, “Probe Option Reference” in *Green Hills Debug Probes User's Guide* for more information.

Probe Configuration Files Automatically Added to Projects and Loaded at Connection to MULTI

When creating a project with the New Project Wizard, if a probe configuration file exists for the target you select, that file will be copied into the new project and will be added to the **Probe Config** tab of the Connection Editor. When you connect to MULTI, the settings in that file will be written to the probe, and will override any current settings on the probe. If you want your probe settings to remain unchanged, you can remove the file from the Connection Editor, and no settings will be written to the probe. If you would like to modify the settings that are written to the probe, you may save your probe's current configuration using the following command:

```
mpadmin -cfgsave probe filename
```

For more information, see “Loading and Saving Configuration Files” in Chapter 1, “Administering Your Probe” in *Green Hills Debug Probes User's Guide* and “Green Hills Debug Probe (mpsrv) Probe Config Settings” in Chapter 3, “Probe Connection Reference” in *Green Hills Debug Probes User's Guide*.

IEEE 1149.7 cJTAG Support for Freescale Targets

The Green Hills Probe now supports reduced-pin IEEE 1149.7 debug modes on Freescale MPC57xx and Kinetis targets. For more information, see the documentation about the **debug_type** option in “Selecting the Target Communication Protocol” in Chapter 4, “Probe Option Reference” in *Green Hills Debug Probes User's Guide*.

For IEEE 1149.7 support for other targets, please contact Green Hills Support.

Support Added for MPC5744P Cut 2

The probe firmware, register definitions, and New Project Wizard entry all now support the Freescale MPC5744P cut 2 silicon.

Improved Support for Freescale Vybrid

The `vybrid` target setting now also debugs the Vybrid's Cortex-M4 core (in addition to the Cortex-A5). Vybrid CPUs that are configured with Cortex-M4 as the primary core can be debugged with the `vybrid.m4pri` target setting.

New Probe Configuration Options

GTL-capable adapters (used for x86 targets) now present a **`use_gtl`** option which can be used to control the use of the GTL drivers. For more information, see **`use_gtl`** in “x86” in Chapter 4, “Probe Option Reference” in *Green Hills Debug Probes User's Guide*.

The probe now allows users to configure how a soft reset is performed on Cortex-A8 targets via the new **`rst_dp113`** configuration option. For more information, see “ARM” in Chapter 4, “Probe Option Reference” in *Green Hills Debug Probes User's Guide*.

Changes in Behavior

`use_swd` Configuration Option Removed

The **`use_swd`** configuration option has been removed. The functionality formerly provided by **`use_swd`** is now available with the **`debug_type`** option. For more information, see “Selecting the Target Communication Protocol” in Chapter 4, “Probe Option Reference” in *Green Hills Debug Probes User's Guide*.

New Syntax for Specifying CoreSight Targets

CoreSight targets are specified using the target setting `csdap()` which describes the set of CoreSight cores and peripherals. Note that the earlier target settings used to specify CoreSight targets will remain in the firmware but are considered deprecated.

When using the new `csdap()` syntax, the probe does not scan the ROM Table to set `cortex_addr`, `etm_addr`, `ptm_addr`, `tpiu_addr` or `tpiu_type`. In addition, the probe no longer automatically detects the index of the AHB-AP, AXI-AP or

APB-AP, but provides new options to specify the index. These options must be correctly set for proper debug operation. In most cases, the **detect** command is able to detect the correct values. For more information, see “Specifying CoreSight Targets” in Chapter 4, “Probe Option Reference” in *Green Hills Debug Probes User's Guide*.

detect Command Changes

The **detect** command now detects several options in addition to `target` and `endianness`. Furthermore, for a target that has a CoreSight DAP, the detected values for `target` use the new syntax described in “Specifying CoreSight Targets” in Chapter 4, “Probe Option Reference” in *Green Hills Debug Probes User's Guide*.

Big Endian Cortex-M Targets Now Supported

Cortex-M targets are now supported in Big Endian data mode. The **inst_endianness** option may be used to select the instruction endianness when in Big Endian data mode.

Removed Features

MPC5746M and MPC5777M e200z0 Core No Longer Available

Debug access to the e200z0 core on MPC5746M and MPC5777M is no longer present in the v5.2 firmware. Contact Green Hills Support if you require debug access to the e200z0 core on these devices.

Chapter 8

Version 5.0.8 Release Notes

Contents

New Features	40
Changes in Behavior	44

This document covers changes to the Green Hills Probe firmware that were added for version 5.0.

New Features

New Supported Targets

Support for the following targets was added in version 5.0.8:

- Cortex-R5 (`cortexr5`)
- Cortex-A15 (`cortexa15`)
- TI OMAP5432 (`omap5`)

Support for the following targets was added in version 5.0.4:

- Cortex-M0+ (`cortexm0`)
- Cortex-A5 (`cortexa5`)
- Freescale Vybrid (`vybrid`)
- Freescale MPC5602P (`ppc560xP.n1`)
- Freescale MPC5602D (`ppc560xB.n1`)
- Freescale MCF 5301x (`mcf5301x`)
- Freescale QorIQ P2041 (`ppcP2041`)
- Freescale QorIQ P5020 (`ppcP5020`)
- Freescale QorIQ P5040 (`ppcP5040`)
- Freescale MPC5744K (`ppc5744K`)
- Freescale MPC5746R (`ppc5746R`)
- Freescale MPC5748G (`ppc5748G`)
- Freescale MPC5777M (`ppc5777M`)
- Fujitsu FCR4 (`fcr4`)
- MIPS 14K (`mips32_14kc, mips32_14kf`)
- MIPS 74K (`mips32_74kc, mips32_74kf`)
- MIPS 1004K (`mips32_1004kc, mips32_1004kf`)

- ST Micro SPC56AP60 (spc56AP60)
- ST Micro SPC570S50 (spc570S50)
- ST Micro SPC572L64 (spc572L64)
- ST Micro SPC574K72 (spc574K72)
- TI AM389x (am389x)
- Xilinx Zynq (cortexa9)

Additional New Project Wizard Support

New Project Wizard support for the following board was added in version 5.0.8:

- TI OMAP5432 uEVM ES2.0 GP

New Project Wizard support for the following boards was added in version 5.0.4:

- Atmel SAMA5 D3x Evaluation Kit
- Freescale iMX6-based targets:
 - Freescale Armadillo 2
 - Boundary Devices Nitrogen 6X
 - Boundary Devices SabreLite
- Freescale Kinetis K20
- Freescale Kinetis K53
- Freescale Kinetis KL25Z
- Freescale MCF53015EVB
- Freescale MPC5744K Demo Board
- Freescale MPC5746R Demo Board
- Freescale MPC5748G Demo Board
- Freescale MPC5777M Demo Board
- Freescale P2041RDB
- Freescale P5020DS
- Freescale P5040DS
- Freescale PX TWR PXD10

- Freescale PX TWR PXD20
- Freescale PX TWR PXN20
- Freescale PX TWR PXR40
- Freescale PX TWR PXS20
- Freescale PX TWR PXS30
- Freescale TWR-VF65GS10 (Vybrid)
- Fujitsu SK-MB9DF125 (Atlas-L)
- Fujitsu SK-MB9EF120 (Calypso)
- ST SPC56AP60
- ST SPC570S50 EVB
- ST SPC574K72 Demo Board
- ST SPC572L64 EVB
- TI AM335x EVM or BeagleBone
- TI RM42 Hercules Development Kit
- TI RM46 Hercules Development Kit
- TI RM48 Hercules Development Kit
- TI TMS570LS31x Hercules Development Kit
- TI TMS570LS12x Hercules Development Kit
- TI TMS570LS04x Hercules Development Kit
- Xilinx Zynq

Support for these boards will be installed into Compiler 2012.1 or newer.

New Trace Support

The SuperTrace Probe v3 now supports debugging and tracing the following targets:

- ColdFire v2, v3, and v4 targets (requires MULTI 6 or newer)
- ARM Cortex targets with a Program Trace Macrocell (PTM) interface, such as the Cortex-A9 (requires MULTI 6 or newer)
- PowerPC 405

- Freescale QorIQ e500mc and e5500 targets, over the high-speed serial trace (HSST) Aurora interface.
- Serial STPv3 can now collect PTM trace on Cortex-A9 targets via the Serial trace interface.

New Support for Target Trace Buffers

This release adds support for embedded trace buffers (ETB) on Cortex-R and Cortex-A targets for which trace is already supported. This feature allows these targets to be traced with a Green Hills Probe, as well as with a SuperTrace Probe v3. See “Supported Devices” in Appendix E, “Supported Devices and Adapter Types” in *Green Hills Debug Probes User's Guide* for information about for more information about which targets have a supported ETB.

AXI-AP Support Added

The probe now supports the AXI-AP bus, which is present on certain Cortex devices. For more information, see “Target-Specific Special Registers” in Chapter 5, “Probe Command Reference” in *Green Hills Debug Probes User's Guide*.

New TraceEverywhere Parallel Trace Interface

This release includes support for a new TraceEverywhere trace pod that supports all existing TE5 adapters and allows the SuperTrace Probe v3 to connect to a much wider set of targets.

Support Through the High-Speed Serial Trace (HSST) Aurora Interface

As of this release, the SuperTrace Probe v3 supports debugging and tracing using the high speed serial trace Aurora interface. This firmware includes support for ARM CoreSight trace on Cortex-R4 and PowerPC Nexus, in both 1 lane and 2 lane configurations.

Probe Run Mode Support

This release adds support for Probe Run Mode for INTEGRITY, allowing targets with live memory access, such as PowerPC and ARM Cortex, to be debugged with a run-mode connection via the JTAG interface without the use of a dedicated serial or Ethernet port on the target, and without halting the target via JTAG. For more information, see “Probe Run Mode” in Chapter 3, “Probe Connection Reference” in *Green Hills Debug Probes User's Guide*.

Faster Power Architecture Trace Decoders

This release includes a new PowerPC 440 and Nexus e200 trace decoders that increase decompression performance and improve reliability. These decoders require MULTI 6 or newer.

New Options for Fujitsu FCR4 Processors

New options have been added to configure the base addresses and size of tightly-coupled memory (TCM). For more information, see “ARM” in Chapter 4, “Probe Option Reference” in *Green Hills Debug Probes User's Guide*.

Programming Spansion SPI Flash Memory Chips from Renesas RZ/A1

Support has been added for programming Spansion SPI flash memory chips from the Renesas RZ/A1. For more information, see “Base Address for Renesas RZ/A1 Flash Chip” in Appendix D, “Troubleshooting and Usage Notes” in *Green Hills Debug Probes User's Guide*.

Changes in Behavior

Changed Use of `trace_clock_phase` Value

The use of `trace_clock_phase` has been updated from previous releases. To calculate the new correct phase, use one of the following equations. If your old setting was greater than or equal to zero:

new_phase = old_phase - 127

otherwise:

new_phase = old_phase + 128

Changed Default of disable_swt Setting

The default for the **disable_swt** setting has changed from `off` to `on`.

Changes to Trace List Options

The **Disable trace when trace retrieved due to trigger** check box in the Trace List options affects the **Retrieve trace when buffer fills** check box, because the **Retrieve trace when buffer fills** feature uses an internal trigger. If **Disable trace when trace retrieved due to trigger** is enabled, trace collection is disabled when the buffer fills up and trace is retrieved. Trace collection will not be automatically re-enabled for the duration of the connection.

To repeatedly fill and retrieve the buffer, disable the **Disable trace when retrieved due to trigger** option.

Defaults For jrst_ and rst_ Commands Changed

The following commands used to default to 300ms, but now default to 10ms:

- **jrst_pulse**
- **jrst_settle**
- **rst_pulse**
- **rst_settle**

New Probe Configuration Files

Some probe configuration files use the new **.ghpcfg** extension. They are similar to **.cfg** files, but are not yet supported in the graphical probe administrator (**gpadmin**). To load a configuration file with **mpadmin**, use the following command:

```
mpadmin -cfgload probe file.ghpcfg
```

MULTI 4 No Longer Supported

The 5.0.8 version of the probe support software no longer supports MULTI 4. If you attempt to install the software on MULTI 4, the 4.4.2 version of the probe firmware and support software will be installed instead.

Chapter 9

Version 4.4.4 Release Notes

Contents

New Features	48
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This document covers changes to the Green Hills Probe firmware that were added for version 4.4.

New Features

New Supported Targets

- Intel Atom (Pineview) (`atom_pv`)
- Intel Atom (Tunnel Creek) (`atom_pv`)
- Intel Sandy Bridge (`sandy_bridge`)
- Freescale i.MX6 (`mx6`)
- Freescale Qorivva MPC560xE (`ppc560xE`)
- Freescale Qorivva MPC564xB (`ppc564xB`)
- Freescale Qorivva MPC564xC (`ppc564xC`)
- Freescale Qorivva MPC567xR (`ppc567xR`)
- Freescale Qorivva MPC5746M (`ppc5746M`)
- Freescale Qorivva MPC5744P (`ppc5744P`)
- Freescale QorIQ P3041 (`ppcP3041`)

Additional New Project Wizard Support

Unless otherwise noted, the following items require MULTI 5.2.4 or newer.

- Freescale Kinetis K70 (requires MULTI 6.1 or newer)
- Freescale MPC560x Demo Board (MPC560xE)
- Freescale MPC564x Demo Board (MPC564xB)
- Freescale MPC564x Demo Board (MPC564xC)
- Freescale MPC567x Demo Board (MPC567xR)
- Freescale MPC5746M Demo Board (MPC5746M) (requires Green Hills Compiler 2012.5.4 or newer)
- Freescale MPC5744P Demo Board (MPC5744P) (requires Green Hills Compiler 2012.5.4 or newer)

- Freescale P3041DS
- STMicro STM3240G-EVAL (STM32F407) (requires MULTI 6.1 or newer)

Support for Reading and Writing MPU Region Descriptors on Freescale MPC57xx

You can now use the **tlbr** and **tlbw** commands to read and write MPU region descriptors on Freescale MPC57xx targets. For example, to limit the first 64KB of SRAM so that it can only be executed in supervisor mode, use:

```
tlbw 0 0x40000000 Inst 0x4000ffff V,Sxsr,W
```

To make sure that it is set correctly, use:

```
tlbr 0
```

or, if you prefer to view all of the MPU entries in a table:

```
tlbr *
```

The probe's representation of the MPU index is as follows:

Probe	MPU
0-5	instruction-only entries 0-5
6-17	data-only entries 0-11
18-23	shared entries 0-5

Support for Cortex-M4F VFP

This release adds support for the Cortex-M4F's VFP floating-point unit. To specify that your Cortex-M has a VFP, suffix the target type with `.vfp` when using the **set target** command.

Parallel Trace Decoding for ETMv3 Targets

This release adds support for ETMv3 parallel trace decoding, which increases trace processing performance for ETMv3 targets. This feature requires MULTI 6.1 or newer.

Chapter 10

Version 4.2.2 Release Notes

Contents

New Features	52
Removed Features	54

This document covers changes to the Green Hills Probe firmware that were added for version 4.2.

New Features

SWD Debug Interface Support

This release adds support for the SWD debug interface. For more information, see the documentation about the **use_swd** option in “ARM” in Chapter 4, “Probe Option Reference” in *Green Hills Debug Probes User's Guide*.

SuperTrace Probe v3 Debug and Trace Support for Additional Interfaces

The SuperTrace Probe v3 now supports debugging and tracing the following targets:

- ARM targets with ETM v3 and CoreSight debug interface
- PowerPC 55xx and 56xx targets with Nexus debug interface

For a list of supported targets, see “Supported Devices” in Appendix E, “Supported Devices and Adapter Types” in the *Green Hills Debug Probes User's Guide*.

BE8 Support for ARM11 and Cortex-R4

The probe now supports BE8 mode for ARM11, Cortex-R4, and the newly-added PJ4 and Cortex-A9 targets. For more information, see the documentation about the **be_mode** option in Chapter 4, “Probe Option Reference” in the *Green Hills Debug Probes User's Guide*.

New Supported Targets for v3 Probes

The Green Hills Probe and SuperTrace Probe v3 now support run control for the following targets:

- Cortex-A9 (`cortexa9`)
- OMAP 4 (`omap4`)

- ARM11MP (`arm11mp`)
- Marvell PJ4 (`pj4_v6`, `pj4_v7`)
- Cortex-M4 (`cortexm4`)
- Freescale Kinetis (`kinetis`)
- Cortex-M0 (`cortexm0`)
- PowerPC 564xA (`ppc564xA`)
- PowerPC 564xL (`ppc564xL_LSM`, `ppc564xL_DPM`)
- PowerPC 564xS (`ppc564xS`)
- PowerPC 567xK (`ppc567xK_LSM`, `ppc567xK_DPM`)
- PowerPC 440GR (`ppc440gr`)
- PowerPC 440EPx (`ppc440epx`)
- PowerPC 440GRx (`ppc440grx`)
- PowerPC 440SPe (`ppc440spe`)
- PowerPC 460GT (`ppc460gt`)
- PowerPC 460EX (`ppc460ex`)
- PowerPC 460GTx (`ppc460gtx`)
- PowerPC 460SX (`ppc460sx`)
- Applied Micro APM82181 (`apm82181`)
- PowerPC 405EX (`ppc405ex`)
- PowerPC 405EZ (`ppc405ez`)
- PowerPC 405EXr (`ppc405exr`)
- QorIQ P1020 (`ppcP1020`)
- QorIQ P1011 (`ppcP1011`)
- PowerPC MPC8308 (`ppc8308`)
- PowerPC MPC5125 (`ppc5125`)
- ColdFire 5441x (`cf54418`)
- Intel Atom (`atom`)
- Intel Core 2 (`core2`)
- Intel Nehalem (`nehalem`)



Note

The `atom` setting is for any Bonnell or Silverthorne device. Processors based on Pineview, Tunnel Creek, or later are not currently supported.

The `nehalem` setting is for any Core i3, i5, i7, or Xeon device based on the Nehalem architecture. Processors based on Sandy Bridge or later are not currently supported.

If you require support for a newer Atom, Core i3, i5, i7, or Xeon processor, contact Green Hills Support.

For a list of supported targets, see “Supported Devices” in Appendix E, “Supported Devices and Adapter Types” in the *Green Hills Debug Probes User's Guide*.

Serial Port Forwarding Now Available

The Green Hills Probe and SuperTrace Probe v3 now support the **pterminal** command, which allows you to connect your target to your probe using the probe's serial port, and initiate a serial terminal session from your host machine over Ethernet.

Removed Features

Diagnostics Pane of Probe Administrator is Not Available in MULTI 6

The **Diagnostics** pane of the **Probe Administrator** will no longer be available after installing MULTI 6 or newer. This pane will continue to be available for MULTI 5.x.

New Online Probe Manuals No Longer Available for MULTI 4.x on Linux

MULTI 4.x on Linux uses a legacy help viewer that does not support newer manuals. If you have MULTI 4.x on Linux, use the PDF documentation instead of the online help.

Chapter 11

Version 4.0.2 Release Notes

Contents

New Features	56
Changes to Existing Features	57

This document covers changes to the Green Hills Probe firmware that were added for version 4.0.2.

New Features

New Supported Targets for v3 Probes

The Green Hills Probe and SuperTrace Probe v3 now support run control for the following targets:

- QorIQ P4040 (ppcP4040)
- QorIQ P4080 (ppcP4080) — Revision 1.x silicon (svr = 0x82080010) is not supported.

For a list of supported targets, see “Supported Devices” in Appendix E, “Supported Devices and Adapter Types” in the *Green Hills Debug Probes User's Guide*.

SuperTrace Probe v3

Green Hills Probe firmware 4.0.2 adds support for the new SuperTrace Probe v3 hardware. This new model features:

- RoHS compliance
- A 4 GB or larger trace buffer
- External Trace Trigger I/O
- USB 2.0
- Gigabit Ethernet

For a list of supported targets, see “Supported Devices” in Appendix E, “Supported Devices and Adapter Types” in the *Green Hills Debug Probes User's Guide*.

selftest Command

The new **selftest** command runs several diagnostic tests on the probe's trace components. It is available on the SuperTrace Probe v3. For more information, see the Green Hills Debug Probes User's Guide.

Changes to Existing Features

Changes to Timestamps

The SuperTrace Probe v3 probe uses a new method to communicate timestamp data to **mpserv**. To collect timestamp data in MULTI from one of these probes, you must update your MULTI installation using the probe installer that ships with this release.

SuperTrace Probe v3 Does Not Have GPIO Pins

The SuperTrace Probe v3 does not have GPIO pins and does not support the **iop** command.

Chapter 12

Version 3.8.2 Release Notes

Contents

New Features	60
Changes and Fixes to Existing Features	61
Deprecated and Removed Features	62

This document covers changes to the Green Hills Probe firmware that were added for version 3.8.2.

New Features

This section lists new features available in version 3.8.2.

Additional PowerPC Support

New PowerPC Processor Support

Supported Processor	Target String
PowerPC 8536	ppc8536
PowerPC 8569	ppc8569
PowerPC 560xB	ppc560xB
PowerPC 560xC	ppc560xC
PowerPC 560xP	ppc560xP
PowerPC 560xS	ppc560xS
PowerPC 563xM	ppc563xM
PowerPC 5668G/E	ppc5668
PowerPC 567xF	ppc5674
QorIQ P2020	ppcP2020

New PowerPC MULTI Project Wizard Entries

The following PowerPC boards are now available for stand-alone projects in the MULTI Project Wizard:

- Freescale MPC8536DS
- Freescale MPC8569-MDS-PB
- Freescale P2020DS

Entries for newly-supported PowerPC 56xx cores will be available in a future release.

TraceEverywhere Cabling System

New probe shipments for some architectures contain TraceEverywhere cabling, designed to provide longer cables with better reliability than the legacy cabling system. Over time, all architectures will be supported over a TraceEverywhere connection.

Changes and Fixes to Existing Features

This section lists changes and fixes to existing features in version 3.8.2.

Updated USB Driver

The 3.8.2 firmware ships with an updated version of the probe USB driver that supports additional operating systems, is easier to install, and is more reliable. This driver supports the following operating systems:

- Windows XP (32-bit)
- Windows Vista (32- and 64-bit)
- Windows 7 (32- and 64-bit)

This new driver is not backwards compatible with earlier versions of some probe software components. These components are updated when you perform a standard install from the probe CD that contains this firmware release.

If you are using Windows 2000, the installer installs the older version of the USB driver.

Probe Now Polls for Adapter and Power Status

If you have configured the probe to detect your target adapter automatically using `set adapter auto`, the probe now updates the setting whenever you plug in or unplug an adapter. It is no longer necessary to type `set adapter auto` or cycle the probe's outputs in order to refresh this setting. Removing an adapter now causes the probe to report an error. The probe also polls to check for the target's power status. The **checker** setting does not affect either of these polling behaviors.

Deprecated and Removed Features

This section lists features that have been deprecated or removed and are no longer supported as of version 3.8.2.

IDT32 Processors Are No Longer Supported

The IDT 32334, IDT 32335, and IDT 32438 processors are no longer supported. The last firmware to support these processors was version 1.4.1.

Chapter 13

Version 3.6.4 Release Notes

Contents

New Features	64
Changes and Fixes to Existing Features	66

This document covers changes to the Green Hills Probe firmware that were added for version 3.6.4.

New Features

This section lists new features available in version 3.6.4.

New ARM Features

Support for New ARM Processors

The following ARM processors are now supported:

Supported Processor	Target String
ARM Cortex-A8	cortexa8
ARM Cortex-M3	cortexm3
Freescale i.MX51 Revision T02	imx51_t02
TI OMAP3	icepick(3:omap3)
TI OMAP2430	omap2430

In addition to supporting these new processors, this release improves support for ARM11, ARM920, and PXA320 processors.

New MULTI Project Wizard ARM Board Entries

The following ARM boards are now available for stand-alone projects in the MULTI Project Wizard:

Board Name	Notes
ARM Evaluation Baseboard Cortex-M3	
Freescale i.MX51 Boards (Babbage and Elvis)	
Logic PD OMAP 3430 Zoom SDK	
TI OMAP 3430 EVM	
TI BeagleBoard OMAP 3530	

Board Name	Notes
ST STM32F10x Evaluation Board	Full stand-alone MULTI flash support

Changes and Fixes to Existing Features

This section lists changes and fixes to existing features in version 3.6.4.

General Changed Features

Additional Commands Supported by gpadmin and mpserve

The **support** and **xswitch** commands are now available in the **Graphical Probe Administrator (gpadmin)** and **mpserve**.

Chapter 14

Version 3.4.1 Release Notes

Contents

New Features	68
Changes and Fixes to Existing Features	71

New Features

This section lists new features available in version 3.4.1.

General New Features

New Probe Commands

The following commands are now available:

Command	Use
support	Prints information useful for Green Hills Support.
xswitch	Sets or modifies internal xswitches. Do not use this command unless instructed to do so by Green Hills Support.

For more information about these commands, see Chapter 5, “Probe Command Reference” in the *Green Hills Debug Probes User's Guide*.

New ColdFire Features

Support for New ColdFire Processors

The following ColdFire processors are now supported:

Supported Processor	Target String
MCF537x family (5372, 5372L, 53721, 5373 and 5373L)	cf5373
MCF5222x family (52221, 52223)	cf52223
MCF5225x family (52252, 52254, 52255, 52256, 52258, 52259)	cf52259
MCF5227x family (52274, 52277)	cf52277
MCF5445x family (54450, 54451, 54452, 54453, 54454, 54455)	cf54455

New MULTI Project Wizard ColdFire Board Entries

The following ColdFire boards are now available for stand-alone projects in the MULTI Project Wizard:

Board Name	Notes
Freescale ColdFire M5373EVB	
Freescale ColdFire M52223EVB	
Freescale ColdFire M52259EVB	
Freescale ColdFire M52277EVB	
Freescale ColdFire M54455EVB	See board_info.txt in your target resources project

New PowerPC Features

Support for New PowerPC Processors

The following PowerPC processors are now supported:

Supported Processor	Target String
PowerPC 8610	ppc8610
PowerPC 8641	ppc8641
PowerPC 8641D	ppc8641D

New MULTI Project Wizard PowerPC Board Entries

The following PowerPC boards are now available for stand-alone projects in the MULTI Project Wizard:

Board Name	Notes
Freescale HPCD 8610	Also known as Lyra
Freescale HPCnet (8641)	Also known as ArgoNavis

New sync_cores Option for PowerPC 8641D

The **sync_cores** option is now available for PowerPC 8641D targets. This option allows you to enable synchronous debugging, for use when debugging a program that shares memory between two cores. For more information, see the documentation for this option in the *Green Hills Debug Probes User's Guide*.

Changes and Fixes to Existing Features

This section lists changes and fixes to existing features in version 3.4.1.

General Changed Features

Changes to `rst_tap_then_sys`

Previous Green Hills Probe firmware releases included an option called **`rst_tap_then_sys`**, which controlled the waveforms generated on the JTAG TAP and CPU reset lines when the target was reset through the probe. This option has been enhanced, and renamed to **`target_reset_pin`**. If you set this option on your probe, consult the following table to determine which value to use for **`target_reset_pin`**.

<code>rst_tap_then_sys</code> Setting	Corresponding <code>target_reset_pin</code> Setting
<code>off</code>	<code>independent</code>
<code>on</code>	<code>freezes_tap</code> or <code>resets_tap</code>

For more information, see “Setting Reset Pin and JTAG TAP Interaction” in Chapter 4, “Probe Option Reference” in the *Green Hills Debug Probes User's Guide*.

ColdFire Changed Features

Improvements to the Detect Command

The **`detect`** command now detects all supported ColdFire processors, except for `cf5206e` and `cf5307`. If you are using one of these processors, set your target string manually.

MIPS Changed Features

EJTAG 2.5 Adapter Power Detection Fixed

The EJTAG 2.5 adapters have been modified to stop reporting erroneous power detection when the adapters were not plugged into a target.

EJTAG 2.5 Targets Ignore `rst_pulse` and `rst_settle`

For EJTAG 2.5 targets, the Green Hills Probe now implements a reset handshaking sequence with the target. Consequently, the `rst_pulse` and `rst_settle` times are ignored. Subsequent releases will give the option of either method.

Detecting External Reset on EJTAG 2.5 Targets

For EJTAG 2.5 targets, the Green Hills Probe now detects when an external (to the probe) reset has occurred by monitoring the `ROCC` bit of the `ECR` debug register.

Changes to the `rr *` Command

For MIPS32 and MIPS64 cores, the registers displayed using the `rr *` command are now limited to those that are available on target variant under test.

PowerPC Changed Features

Probe No Longer Sets MSR[SPE] After Target Reset

For PowerPC 55xx targets, the probe no longer sets the `MSR[SPE]` bit after target reset. If your application requires this bit to be set, you may set it in your setup script or in the appropriate target initialization code.

eTPU Is Available for Debugging

For PowerPC 55xx processors that have an eTPU, the probe now makes the eTPU available for debug as an additional core. For example, if debugging an MPC5553, the 5553 will be core 0, and its eTPU will be available as core 1.

MSR[SPE] Bit Not Set During Reset Sequence

Firmware previous to version 3.0.0 supporting MPC85xx processors set the `MSR[SPE]` bit as part of the reset sequence. In firmware 3.0.0 and higher, that no longer happens, and the `MSR[SPE]` bit remains 0 at reset. If your application requires the `MSR[SPE]` bit to be set, you may have to set it in your setup script, or set it in your initialization code, for proper operation. Also note that the probe's `vc` diagnostic tests require the `MSR[SPE]` bit to be set and will not pass otherwise.

Chapter 15

Known Issues and Limitations

Contents

General Known Issues	76
ARM Known Issues	85
ColdFire Known Issues	96
MIPS Known Issues	97
Power Architecture Known Issues	99
x86 Known Issues	106

This chapter lists known issues and limitations with the current probe release.

General Known Issues

Cache Visibility Features Show No Data in MULTI

In some rare cases, cache visibility (**cacheview** and **cachefind** commands) may not work in MULTI on targets that normally support this feature. To restore cache visibility, disconnect and then reconnect **mpserv**.

Cannot Downgrade Firmware On Some Probes

Due to a manufacturing change, probes with serial numbers 15000 - 15299 and probes with serial numbers greater than 15500 require firmware 3.6.4 or higher. The firmware on these probes cannot be downgraded to an earlier version.

Installation Disables ecomarm2 License

If, after installing your probe software, **ecomarm2.exe** cannot obtain a license:

1. Navigate to your MULTI install directory.
2. Rename **ecomarm.exe** to **ecomarm.old**.
3. Rename **ecomarm2.exe** to **ecomarm.exe**.
4. Run `update.exe -i -f filename.lck -na ecomarm`.
5. Rename **ecomarm.exe** back to **ecomarm2.exe**.
6. Rename **ecomarm.old** back to **ecomarm.exe**.

USB Driver Installation Fails on Windows Vista

If USB driver installation fails on Windows Vista and you see a dialog box with the following message:

Windows encountered a problem installing the driver software for your device

1. Reboot your computer.

2. Run ***install_dir*/driver/drivertool.exe**.
3. Click **Install Driver**.

The second installation should work without any errors.

Green Hills Probe v4 Requires mpadmin Included with Probe 6.0 CD or Later

If you attempt to update a Green Hills Probe v4 using an older version of **mpadmin**, you may get an error that approximates the following:

```
You have a GHS Probe Version 1 (ARM), but this firmware file does not contain  
an image for that version.
```

This message indicates that you are using an outdated version of **mpadmin**. Use the version that came with your version 6.0 CD (or later).

General Issues Updating Probe Firmware

If you encounter an error updating firmware on your probe:

1. Try updating again.
2. Reboot the probe and try updating the firmware again.
3. If the same error persists, contact Green Hills Support.

This is most likely to occur with probes that have serial numbers between 10001 and 10120, and may also happen with probes that are being updated from a firmware version earlier than 5.0.2.

Probe Cannot Update Directly from Pre-4.4 Firmware

Probe firmware versions prior to 4.4 will not directly update to probe firmware version 5.4 or later. Instead, **mpadmin** will automatically perform a two-step update using an installed **recovery.frm** as an intermediate firmware. The two-step update can be performed manually (but not automatically) using the Graphical Probe Administrator: update to **recovery.frm**, then update to the latest firmware you have available. The **recovery.frm** file is located in ***install_dir*/ghprobe/**.

Connecting to Multiple USB Probes via the Probe Administrator

If multiple probes are attached to a PC via USB, it will not be possible to specify a connection to any such probe by using the **Add New Probe** option in the Probe Administrator. Instead, run the Probe Administrator from the command line:

```
gpadmin -usb serial_number
```

where *serial_number* is the serial number of the probe you want to connect to.

Green Hills Probe v4 USB Connections to Virtual Machines

Virtualization software may have USB compatibility issues with Green Hills Probe v4. We recommend that you use only Ethernet connections with virtualized operating systems.

Green Hills Probe v4 Does Not Support Simultaneous pterminal Connections

Green Hills Probe v4 supports serial port forwarding of USB devices that may enumerate multiple serial ports. However, only one **pterminal** connection can be operable at any time. Any extant connection must be closed prior to establishing another.

USB-Serial Device Disconnections May Be Silent

If a USB-Serial device is disconnected from a probe while it is in use, or if the front panel USB port is powered off, no notice will be given on the **pterminal** console. To restore the serial connection, you must close **pterminal**, reconnect the USB-Serial device, and then restart **pterminal**.

Unresponsive or Unreliable Network Connection

If you experience an unreliable or unresponsive network connection to your probe, ensure that it is connected to your network via the rear LAN port. If it is connected via the front LAN port, the connection will only be functional while the rear LAN port is active.

Errant Output from pterminal Session

During an active **pterminal** session, some USB changes are unsupported and may result in unpredictable serial output:

- Disconnecting and reconnecting a USB serial adapter from the probe's front panel.
- Powering off the probe's front panel USB port during an active **pterminal** session.

To ensure correct behavior after reconnecting a USB serial adapter, exit from **pterminal** (press Enter followed by ~ and .) and run the **pterminal** command again.

Delayed pterminal Characters

When running commands (such as **tr**) from a different probe console while using **pterminal**, characters typed at the **pterminal** console will be delayed until the other command has finished.

Issues Interleaving MULTI Script and mpserve Commands

In certain situations, if you issue a run-control command to **mpserv** after a MULTI run-control command, MULTI may not report the correct status of your target. This may cause a subsequent command to fail.

For example, if you issue the following commands in a board setup (**.mbs**) script or the MULTI Debugger's **cmd** pane:

```
>halt  
>target run
```

and then hit a breakpoint, `target tc` may not cause the target to run, even in cases where the probe reports the target as halted. To work around this scenario, do not interleave MULTI script commands with debug server run-control commands. This issue is under investigation and will be addressed in a future release.

Probe Administration Prompt Pane May Desynchronize After detect Command

After running the **detect** command, the target type reported in the **Prompt** pane of the **Probe Administration** window may not update. This can happen regardless of whether **detect** is manually input into the Prompt pane or triggered via the **Detect** button in the **Configuration** pane. To force a refresh, enter the following in the **Prompt** pane:

```
t 0
set target
```

Some Tabs Are Empty in the Register View Window

Some peripherals are not initialized by the default setup script. If you attempt to access an uninitialized peripheral, you can put the target in a bad state. For this reason, registers that are not initialized are sometimes marked *hidden* in the register definition (.grd) file, and do not display in the **Register View** window. In some cases, an entire group of registers is hidden, so the tab for that group in the **Register View** window is empty. To view these registers, make the following modifications to your .grd file:

1. Look for registers with the attribute `hide = ${FLAG}`
2. Change the value of *FLAG* to `false` to show all registers marked with that flag.

target tc and target th Behavior Changes when Halt Cores Synchronously is Selected

When the **Halt Cores Synchronously** mpserve connection option is selected, the behavior of the **target tc** and **target th** commands changes.

- **target tc** changes a core's status from `Stopped` to `Paused`. If all other cores are `Paused`, `MULTI` runs all cores.
- Similarly, **target th** changes a core's status to `Stopped`. If any other cores were running, `MULTI` changes their status to `Paused`.

You may need to modify your setup script if it contains **target tc** or **target th** commands that are directed to specific cores via the **t** command (e.g., `target t 3..4 th`). Instead of using **target tc** or **target th**, use `groupaction -r @all` to resume all cores and `groupaction -h @all` to halt all cores.

Incorrect Trace Decoding

If you disable and then reenable trace before all collected trace data is retrieved, data in subsequent retrievals may be incorrectly decoded. To work around this problem, either wait for trace to be completely decoded before reenabling trace, or clear trace after disabling and prior to reenabling trace. This limitation affects MULTI 7.x and earlier.

Errors While Changing Trace Options on Multi-Core Targets

In MULTI 7 or earlier, changing trace options on a multi-core target can—in rare cases—cause application errors. Before changing trace options, we recommend disabling and clearing trace first.

Changing Trace Options While Tracing May Result in Incorrect Trace Decoding on MULTI 7 and Earlier

Changing options in the **Trace Options** window while trace is enabled may result in trace being decoded incorrectly. To work around this, first disable trace, then change any options, then reenable trace.

Break on Trigger Only Halts Target If Target is Not Already Halted

If you use the target-specific **Break on Trigger** trace option, the probe does not halt the target if the target is already halted when the trigger is hit. On ETM targets, if you have enabled this setting, have an execute trigger set on an address range, and are halted in that range, the trigger occurs immediately; the probe does not halt the target after you run.

Setting Options in the Trace Options Window Has No Effect When Data Trace is Disabled

When **Data Trace** is not enabled in the **Trace Triggers** window, MULTI will still allow you to select different **Data Capture** modes in the **Trace Options** window, but data trace will not be collected.

Gap Between Timestamps in the Trace List or Path Analyzer

When the host buffer is full, MULTI attempts to discard unnecessary trace data. This behavior may cause side effects as buffers are discarded over time, such as a gap when viewing timestamps in the PathAnalyzer or Trace List.

Trace Data Lost when Trace is Disabled Immediately After Retrieval

When controlling trace operations through a MULTI script, trace data collected while the target was running may be lost due to a race condition when trace is turned off, trace data retrieved, trace is turned on, and the target is run.

Because it is a race condition, this issue only occurs when these commands are run consecutively in a setup script; it does not occur when you execute these commands manually. To work around this issue, insert `wait -time 1000` command between trace retrieval and turning trace on.

AddressSpaces Not Traced by Default After Disabling Trace

When you right-click any AddressSpace in the Debugger's target list and clear the **Trace** menu item, subsequently created AddressSpaces are not traced by default. To work around this issue, manually activate trace for new AddressSpaces.

TimeMachine Demo Requires Specific Trace Options

In order to run the TimeMachine demo, you must select the following options in the **Trace Options** window:

- **Automatically enable trace collection**
- **Retrieve trace when target halts**

- **Retrieve trace when buffer fills**

Modifying Target State While Tracing May Cause Incorrect Memory or Register Reconstruction

Trace is used to reconstruct registers and/or memory in TimeMachine mode. If you halt the target while trace is being collected and modify memory or registers in any way (including via a command line procedure call), their reported values may be incorrect in TimeMachine. To work around this issue, do not modify memory or registers while collecting trace.

Tracing a Program Running from ROM with a Setup Script

When running out of ROM while using a setup script and trace enabled, the probe will trace the action of the setup script, which may result in decompression errors. To resolve this, issue **trace clear** after running the **setup** command. You can also add **trace clear** to the end of your setup script.

Target's Cores May Have Desynchronized Trace Timestamps

If you capture trace from a core that was not traced in an early capture, timestamps may not be synchronized between all cores. To work around this issue, ensure that all trace captures use an identical set of cores while debugging.

Timestamps May Overflow After 213 Days of Uptime

Calculated timestamps can overflow every 2^{64} picoseconds (about 213 days). Counters are reset every power cycle. To work around this issue, cycle the power of the target (if the target is generating timestamps) or the probe (if the probe is generating timestamps) at least once within 213 days of collecting timestamped trace.

Trace Clear May Disable Trace Collection on MULTI 6

When tracing a target using MULTI 6.x, it is possible for a "trace clear" operation to disable trace collection, even though the GUI will show trace as enabled. This is a rare event. To resolve this issue, disable and then reenables trace collection.

Entering and Leaving Debug Mode May Interfere with a Trace Disabled Packet

When trace is filtered using the **Trace Triggers** window, a **Trace Disabled** packet may not be correctly output. This can occur in two cases:

1. Starting from debug mode in an address range that is not traced.
2. Tracing up to debug mode in an address range that is not traced.

In these cases, TimeMachine may show incorrect reconstructed values. This limitation affects all trace architectures and trace capture methods.

TE Pod logic_high Setting

TE Pods through Revision D (serial numbers less than 1000) cannot reliably drive the following pins of the following adapters when the setting for `logic_high` is greater than 3.5 volts. These pins will still continue to function as inputs.

- MIPI-34 — `DBGACK` and `nTRST_PD`
- MIPI-60 — `TRIGOUT` and `TRST_PD`
- Nexus-HS22 — `EVTI`
- Nexus-HS34 — `GEN_IO3` and `GEN_IO5`
- Nexus-HS70 — `EVTI`
- Nexus-HP50 — `BOOTCFG` and `TOOLIO5`
- Nexus-MICTOR — `BOOTCFG`
- MIPS-PDTrace-MICTOR — `TR_TRIGOUT` and `TR_PROBE_N`
- TI14 — `EMU0`

If `logic_high` is set above 3.5V and an affected TE Pod is in use, any affected pins will automatically be tri-stated. If any of these pins need to be driven, set

`logic_high` to 3.5V or lower. Most targets that use a `logic_high` above 3.5V will work properly with a `logic_high` setting of 3.5V. You must reboot your probe or reconnect your adapter if you change `logic_high` within the supported range after a pin had been tri-stated.

Enabling Outputs Does Not Report an Error with Incorrect TE Adapter Setting

When the `adapter` setting is not set to `auto` and you connect a TE Adapter, the probe's outputs will be tri-stated and cannot be reenabled until the `adapter` setting is changed to `auto`. Neither of the two methods of enabling outputs (**jp on** command, or pressing the **user** button when `user_button` configuration option is set to tri-state) will reflect this error, and it will appear to succeed even though outputs remain tri-stated.

ARM Known Issues

Cannot View I-Cache or L2 Cache on Cortex-A5 Targets

For Cortex-A5 targets, the MULTI **Cacheview** window allows you to select I-cache and L2 cache, but no data is available or will be displayed for these caches.

Cannot Debug Certain Cache Configurations on Cortex-A5 and Cortex-A9 Targets

The probe is unable to step off breakpoints on Cortex-A5 and Cortex-A9 targets when the L1 I-cache is enabled, L1 D-cache is disabled and the L2 cache is enabled. If the L1 D-cache is disabled, then the L2 cache must also be disabled or debug features including (but not limited to) software breakpoints may be disabled or unreliable.

Issues Debugging the M4F Cores on i.MX8 QM and QXP While Caches are Enabled

We do not recommend debugging the M4F cores on i.MX8 QM and QXP while their caches are enabled. If doing so is critical to your project, you must manually invalidate the caches prior to downloading code (if there is a download process), and debug only with hardware breakpoints. Note that modifying opcodes and setting/removing software breakpoints will not work because probe management of the caches has not yet been implemented for these i.MX8-M4F cores.

This issue will be fixed in a forthcoming release and does not apply to the Cortex-A cores on the i.MX8.

Many TMS570 and R4x Processors Incorrectly Detected as a Cortex-R4F

Many TMS570 and R4x boards are incorrectly detected as a Cortex-R4F. If you have one of these targets connected to the probe, run the following commands to configure the probe correctly:

```
> dlh
> detect
> set target icepick(0:cortexr4)
```

No Access to XScale Cache Operations Register

The probe does not implement access to XScale coprocessor 15 register 7 (the cache operations register), but when it writes to the target's memory, it flushes the I-cache lines and cleans the D-cache lines to which the memory write maps. It also flushes the write buffer before resuming the target. That said, the lack of explicit cache invalidate, clean, and allocate commands may make it difficult to set up a bare board. Contact Green Hills Support for information about when these facilities will be implemented.

bl Displays Duplicate Breakpoints

Under certain conditions, the **bl** command displays duplicate entries for breakpoints. These duplicates do not indicate a problem, and can be ignored.

Slow Halt On ARM920 Target

Halting an ARM920 with a slow JTAG clock and caches enabled may take a long time. This problem is most frequent with an AT91RM9200 running an application in ROM. To increase speed, configure the probe with the following command:

```
xswitch -tmpl_arm7_arm9.upload_arm920_dcache_on_halt
```

When using this setting, **Cacheview** does not work.

Trigger Immediately Causes Two Triggers on CoreSight ETM11 Target

Due to a workaround for ARM erratum 350999 that affects CoreSight ETM11, using **Trigger Immediately** on an ETMv3.2 target may result in two triggers.

Triggers During Overflow May Be Dropped

Some ARM trace targets output triggers such that they will be lost if they occur near an overflow. These targets will not trigger reliably when there are trace overflows. For more information, consult the ARM core TRM.

Cannot Collect Trace Data on a Trigger on OMAP3

Because the TI OMAP3 does not connect the ETM trigger to the TPIU trigger output, the SuperTrace Probe cannot collect data on a trigger on this target.

Freescale i.MX51 Does Not Work at Slow Clock Speeds

The Freescale i.MX51 may not work reliably with TCK speeds slower than 8 kHz. It does work reliably at higher speeds. To work around this issue, use a higher clock speed.

Some ETMv4 Features Are Not Supported

The following ETMv4 features are not currently supported: context ID comparators, virtual machine ID comparators, and Q elements.

ETMv4 Triggers That Combine Execute Comparators with Data Access Comparators Are Not Reliable

Due to speculative execution, a trigger may fail if it uses a Boolean AND to combine the following:

- Execute address (single or range).
- Data read/write address (and, optionally, value).

This can apply even when the data is accessed while executing instructions in the given address range. (The execute comparator and data comparator may not fire on the same cycle.)

To partially work around this issue, do the following: First, create a state machine that enters an active state when instructions in the address range are executed and enters an inactive state for out-of-range execution. Second, combine the state machine with the data comparator. This workaround is only partial because the relevant data access may still be done speculatively while the state machine is in an inactive state.

Probe `etm_register` Options Must Be Manually Set on Multi-Core ETMv3 Targets

If you intend to trace a multi-core target with ETMv3 cores, the various `etm_register` options must be manually set for all cores. The probe tools may not automatically access ETM registers on all cores to determine trace capabilities. For more information about `etm_register` options, see the relevant table cell in “Target-Specific Configuration Options” in Chapter 4, “Probe Option Reference” in *Green Hills Debug Probes User's Guide*.

Trace Count for Accesses to or Execution of a Single Address on ETM Targets

For ETM trace, if you are counting accesses to or execution of a single address with a count, the count is exact. It counts the number of times the address was accessed or executed. If you are counting accesses to or execution within an address range or a symbol the count is sticky. It counts the number of cycles between access or execution of an address in the range and access or execution of an address outside

the range. For practical purposes, this means that using a count with an address range is unlikely to yield the desired results.

Trace May Not Decode Correctly While Booting Cortex-A INTEGRITY Systems

If the trace system is enabled while a Cortex-A INTEGRITY system is booting by download, it will collect trace data of boot loader execution and secondary core spin loops in the boot MMU configuration, which may not match the MMU mappings used after the kernel is up and running. If this happens, the affected portion of the trace buffer will not decode correctly and may abort and/or cause errant memory reads from the target if the corresponding trace decode options are enabled.

To work around this issue, disable trace until after secondary cores are booted during BSP initialization. An alternative workaround is to disable decoding abort on opcode failure and reading unknown opcodes from the target, and disregard the incorrect portion of the trace buffer which occurs before secondary core initialization.

Missed Trace Triggers in INTEGRITY Virtual AddressSpaces

On the AT91RM9200, a trace trigger may be missed if trace is disabled in an INTEGRITY virtual AddressSpace while the trigger condition is met in that AddressSpace. To work around this issue, re-apply trigger settings or re-enable trace after modifying which address spaces are traced.

Some ARM Cores Must Be Halted When Enabling Trace

Some ARM cores, such as the ARM1156, ARM1176, and PJ-4, must be halted when trace is enabled. If you are using one of these cores, either:

- Enable trace manually, only when the core is halted, or
- pass the **-Xetm_halt_to_trace** argument to **mpserv**. This command halts and then resumes the target as needed when enabling trace.

ARM ETMv1 and ETMv3 64-Bit Data Accesses Displayed as 32-Bit Accesses in Trace List

When tracing ARM ETM targets, the Trace List displays 64-bit data accesses as two 32-bit accesses. This issue does not affect ETMv4 targets.

Insufficient Trace Bandwidth for R-Car Evaluation Boards

Certain R-Car gen3 evaluation boards may have insufficient trace bandwidth to perform ETM trace of all cores running INTEGRITY SMP. This bandwidth issue is most pronounced on the Salvator-XS H3/M3 boards, but may be evident on other boards in the same family. If there is not enough bandwidth, ETM output FIFO overflows will occur which can interfere with TimeMachine analysis tools. The required bandwidth is proportional to the number of instructions executed per second, and the available bandwidth is connected to the number of PCIe lanes switched to HSSTP trace.

Available bandwidth:

- Salvator-XS H3/M3 — 1 PCIe lane, 4Gbps
- Condor V3H — 2 PCIe lanes, 8Gbps
- Draak D3 — 4x LVDS, approximately 3Gbps total
- Eagle V3M — 4x LVDS, approximately 2.8Gbps total

CPU Cores for INTEGRITY:

- Salvator-XS H3 — 8 total: 4x A57, 4x A53
- Salvator-XS M3 — 6 total: 2x A57, 4x A53
- Condor V3H — 4x A53
- Draak D3 — 1x A53
- Eagle V3M — 2x A53

Each A57 core at default clock rates requires 2-3Gbps of ETM trace bandwidth, while each A53 core requires approximately 1Gbps. Note that trace bandwidth is highly variable and depends on both the code loaded on the system and system activity levels. On the A53 cores, the **Stall Processor to Avoid Overflows** option may be available to reduce the frequency of FIFO overflows at the expense of

real-time system performance. On the A57, this option is not available, but reducing the CPU core clock or enabling trace only on a subset of cores may be sufficient to match ETM output bandwidth to the available trace capabilities. A custom board built for H3 or M3 might also have the option of using 2 PCIe lanes for HSSTP trace to double available bandwidth.

Probe Cannot Detect Some ICEPick Targets

If your target has an ICEPick, and there is a device on the JTAG scan chain that is not controlled by the ICEPick, the probe's **detect** command will not be able to detect your target.

Some Data Missing from Trace Buffer on Cortex-M3 Targets

Some Cortex-M3 targets do not properly flush all trace to the SuperTrace Probe when halting. Due to this issue, small amounts of data from the end of the trace buffer may not be captured. To reduce the frequency of this issue, use a larger port size.

Some ARM11 CPUs Cause Incorrect Trace Data

Some ARM11 CPUs, including the Freescale i.MX31, contain a hardware erratum that can cause trace errors and incorrect trace when tracing execution in Virtual AddressSpaces. For more information, see ARM erratum 351599.

Break on Trigger Does Not Trace Final Instruction on Cortex-R4

When the **Break on Trigger** check box is enabled, some Cortex-R4 targets do not trace the final instruction before halting due to a trigger.

Enabling Trace on Multiple Running Cores

Multi-core trace on ARM targets is enabled on each core sequentially. This means that if one or more cores are running when trace is enabled, you will capture a small amount of trace of the first enabled core before capturing any trace from the next one, and so on. If you are using a small trace capture buffer (such as ETB) and

retrieving trace when the buffer fills or due to a trigger, you may fill your buffer or hit your trigger condition prior to trace being enabled on all cores. This can result in no trace being captured for some cores. One workaround is to halt cores you want to trace prior to enabling trace. Another is to choose your triggers with this behavior in mind, or manually enable/disable trace.

ARM Multi-Core Trace Targets with MULTI 6.x and Earlier May Require Enabling Trace Manually

Multi-core trace on ARM targets requires access to trace registers on each core when trace is initialized after the setup script is run. If your setup script does not enable access to those registers on all cores, trace will not be automatically enabled on those cores, and you may see the error message `Debug server failed to connect to TraceServ`. When the trace registers are available, you can manually initialize trace on those cores by taking a trace action (such as opening a trace window like the Trace List or Trace Options window).

At that time, if the check box **Automatically enable trace collection** is selected, trace will be initialized again, which may cause problems if you are currently collecting or retrieving trace on another core. We recommend clearing that check box and manually enabling trace. When manually enabling trace, first download to all cores, initialize trace on all cores, and then enable trace.

Tracing ARM Targets Triggering Close to the Beginning of the Trace Buffer

ETM and PTM trace (all versions) output a periodic synchronization sequence, generally every 1024 bytes of trace. When decompressing trace, everything prior to the first synchronization sequence is discarded. If your trace buffer size and trigger position are configured so the trigger might be in the first 1024 bytes of the buffer, trace will still trigger and collect, however there may be no indication of the trigger position in the decompressed trace if it was discarded prior to the first synchronization sequence.

Function and Callees Filter Issue

On a Cortex-A9, if you create a trace filter using **Trace on: Function and Callees Executing**, the first instructions of the specified function (up to and including the first branch) might not be traced.

SWD May be Unreliable on Freescale Vybrid

The Green Hills Probe cannot reliably debug a Freescale Vybrid using SWD. To work around this issue, use JTAG to debug Freescale Vybrid SoCs. For more information, see “Selecting the Target Communication Protocol” in Chapter 4, “Probe Option Reference” in *Green Hills Debug Probes User's Guide*, or contact Green Hills Support.

Flash Programming May Be Unreliable on Renesas RZ/A1 Board

Writing to flash on the Renesas RZ/A1 board may be unreliable with gflash. If a write failure occurs, erase the flash, and try the write again. The second write will usually work, but in the rare case that it also fails, a third attempt will succeed.

Data Trace of Load/Store Multiple Instructions on ARM Targets with ETMv3.x with Incomplete Data

In some cases, a Load/Store Multiple instruction will not output trace packets for all data transactions that occurred. In this case, TimeMachine will treat the data transactions that were output as the last transactions. For example, if you trace an LDM instruction that loads data into registers R3, R4, and R5, but there are only two traced data transactions, those data transactions will be traced as having been loaded into R4 and R5. This behavior is as specified in the ETMv3 specification, but there are cases where hardware does not behave according to the specification that can result in incorrect TimeMachine memory and register reconstruction.

If you encounter a case where a Load/Store Multiple instruction is traced, some but not all of the data transactions are traced, and the reconstructed values appear to be incorrect, please contact support.

AArch32 Debug Not Supported

Debugging targets with ARMv8-A processors while running in AArch32 mode is not supported. If you require this feature, please contact Green Hills Support.

Issues Upgrading to Firmware 5.2

If you are experiencing issues during or after upgrading to firmware 5.2, please check the following:

1. The setting for **l2_cache_present** and **l2_cache_address**.

While it has always been important to correctly set **l2_cache_address** and **l2_cache_present** on Cortex-A5 and Cortex-A9 processors, firmware 5.2 is especially reliant on these options. As a result, if these options are set incorrectly you will experience a host of negative symptoms, such as the target failing to halt at a software breakpoint, failing to step off of a software breakpoint, or failing to resume from the address of a recently cleared software breakpoint.

2. The settings for **rst_pulse**, **rst_settle**, **jrst_pulse**, and **jrst_settle**.

The above options specify the times of certain parts of the target reset process. However, probe overhead sometimes causes longer delays than specified. Firmware 5.2 significantly reduced probe overhead during the reset of CoreSight systems. If your target has been using small values for those options, it may have been inadvertently relying on the probe's internal overhead to generate longer delays. After upgrading to firmware 5.2, you may need to increase these times in order to reliably reset. For more information, see Chapter 4, “Probe Option Reference” in *Green Hills Debug Probes User's Guide*.

ARMv7 Trace

Trace does not include task information when tracing an INTEGRITY BSP that uses the ARMv7 ASP.

Trace May Not Reconstruct Canceling Exceptions on ETM Targets

In some cases, a canceling exception on ARMv7 targets may cause the decoder to lose synchronization for PC trace. A canceling exception packet may cause the decoder to branch to an address outside the program due to misinterpreting prior P-headers and exception return packets. On ARMv7-M targets specifically, the decoder may fail to reconstruct tail-chained exception handlers.

Trace to the ETB with Triggers is Limited on the Vybrid

Due to a hardware limitation, the Vybrid ETB does not acknowledge triggers. After a single trigger has occurred and trace collection has stopped, it is not possible to restart collection without a system reset. Further attempts to collect trace from the ETB will result in invalid data being returned.

On ARM11, Instruction-Executed Trace Triggers May Trigger While Halted

While halted, debug operations on ARM11 are accomplished by instruction stuffing. The PC increments with each debug operation, and the CPU appears to be executing instructions to the trace system. Because of this, if you halt at an address close to an address you want to trigger on, debug operations may cause the PC to increment to the trigger address. This will result in the trace system triggering even though the instruction in question did not execute.

ETMv3 Parallel Trace Decoding Limitation

Parallel trace decoding is not supported when tracing targets with multiple traceable cores. To trace only one core and enable parallel trace decoding, specify the core with `-force_trace_coreid`. For more information about `-force_trace_coreid`, see “Options for Custom Connection Methods” in *Green Hills Debug Probes User's Guide*.

Legacy ARM-20 Adapter Ignores Vref

Legacy ARM-20 adapters (for the Green Hills Probe) only use Pin 2 (`Vsupply`) for power detection instead of Pin 1 (`Vref`). If your board does not connect power

to Pin 2, power detection and the **dlh** command will not work and the **power_detect** option must be turned off.

ColdFire Known Issues

Power Detection Limitations

Power detection is not supported for the 5235, 5271, and 5275. When using these processors, turn off power detection with the following probe command:

```
set power_detect off
```

Breakpoint Limitations

Breakpoints on virtual tasks or virtual memory areas are not supported.

Detecting a ColdFire Target with SuperTrace Probe

To detect a ColdFire target with a SuperTrace Probe, the target should first be set to a ColdFire target before issuing the **detect** command. For example, the following sequence will work reliably:

```
jp off  
set target cf5249  
detect
```

If the target is not set to a ColdFire, the SuperTrace Probe will attempt JTAG detection, which does not work with ColdFire targets. The Green Hills Probe does not have this limitation.

Problems Capturing Triggers on ColdFire V4 Targets

If you set a trigger on a ColdFire V4 target and find that the trigger is not being reported, try the following procedure:

1. Disable trace (MULTI command: `trace off`).
2. Download your program (MULTI command: `prepare target -load`).

3. Enable trace (MULTI command: `trace on`).
4. Resume your program (command: `c`).

Changing the trace configuration after starting the program, or performing a trace clear operation, may require repeating the above procedure to properly enable triggers.

This note only applies if you are downloading your program.

Undefined Behavior When Using the jp Command and the ColdFire Active Pod for GHP3

When using the GHP3 and the ColdFire Active Pod, the **jp** command's pin-specific drive mode arguments are not supported. Employing the command arguments will lead to undefined behavior of the modified pins. The ColdFire Active Pod has pin-appropriate drive modes built-in to the device.

MIPS Known Issues

freeze_timers Disables the EN Bit in CTC1, CTC2, and CTC3

For IDT32438 targets, the **freeze_timers** option will freeze the core's general-purpose 32-bit counter/timers by disabling the **EN** bit in **CTC0**, **CTC1**, and **CTC2** while the target is in debug mode. When this option is enabled, any attempts to access these memory-mapped registers will not give the desired result. If you want to write to them, you must ensure that the **freeze_timers** option is off when the target is halted right before accessing these registers, or off when the target is run right after accessing these registers.

Low Level JTAG Procedures May Disrupt M4K Processors

When debugging an M4K processor, some low level JTAG procedures may disrupt the processor for a short time, causing problems with run control. The **detect** command is an example. This issue is being investigated, and should not cause problems during normal debugging.

Stepping Off of Breakpoints May Not Work When Debugging a Virtual Task

When debugging a virtual task (for example, using OSA), stepping off of a breakpoint may not work. If you encounter this problem, launch **mpserv** with the **-X_virtualPPC** argument.

Accessible Physical Address Range Limited to 512 MB

The Green Hills Probe accesses physical memory on MIPS through a 512 MB window at 0xa0000000 or 0xffffffffa0000000. This corresponds to a physical address range between 0x00000000 and 0x1fffffffff. Accesses outside the range fail, causing the probe to print the following error to the console:

```
ERROR 55 (memory read error): Memory read failed ERROR 14 (invalid parameter):  
Currently physical addresses greater than 0x20000000 are not supported.
```

If you are debugging a kernel that references addresses outside this range, OSA support in the MULTI Debugger may also be limited.

This issue affects all firmware revisions from 3.0.0 to the current release.

TC Restrictions on MIPS 34K and 1004K Processors

The setup script activates only the first TC of each core on MIPS 34K and 1004K processors. Also, **mpserv** will not allow programs to be downloaded to RAM using alternate TCs. To work around this, use the first TC to download and run programs. The program running on the first TC should configure and activate alternate TCs.

Halt Cores Synchronously Not Supported with Multiple Subsets of Cores on MIPS

On MIPS targets, when the **Halt cores synchronously (-synccores)** mpserv option is used with a subset of cores selected with the **Debug these cores (-force_coreid)** option, connecting to another mpserv with **Halt cores synchronously** to another subset of cores at the same time is not supported.

Power Architecture Known Issues

Incorrect Trace Decoding on PPC405 Processors

If the first broadcast in a trace capture is one of the following, trace decoding may provide incorrect data:

- INTEGRITY TaskContext information branch
- `mtctr`
- `mtlcr`
- `sync`

If you run into this issue, contact Green Hills Support.

MPC5744P Stalls with Certain Trace Settings

The MPC5744P may stall indefinitely when:

- **Stall Processor to Avoid Overflows** is set to `on`
- **Use Branch History Messages** is set to `off`
- **Trace Clock Multiplier** is set to `1/1x`

We recommend enabling branch history messages or using a `1/2x` trace clock multiplier when tracing this target.

Incorrect Trace with PowerPC e200 and MULTI 6

When tracing a PowerPC e200 target with MULTI 6, if you are using the **Trace on:** feature, the instructions shown for the beginning of trace after the `start` event may be incorrect. This may also result in trace errors. The instructions become correct again after a direct branch, or if branch history mode is enabled, after an indirect branch. This issue has been fixed as of MULTI 7.

Censorship Unlock Requires Two Resets on PPC560x Processors

When using the probe's **censor_unlock** option to unlock a PPC560x target, the probe may need to reset the target twice in order for the unlock to succeed.

Little Endian Mode Is Not Supported on PowerPC e500-, e500mc-, e5500-, or e6500-based Targets

Little endian mode is not currently supported on PowerPC e500-, e500mc-, e5500-, or e6500-based targets.

Incorrect PC Location After Halting Target

On PowerPC 603, 7xx, 5200, and 82xx, processors, if the processor is spinning at a branch-to-self opcode (0x48000000) that is in memory as the last instruction in an I-cache line (for example, at an address ending with 0x1c or 0x3c), and the I-cache is enabled, then halting the processor may result in a reported PC that is four bytes past the true PC. This happens as a result of branch folding, and is currently being investigated with Freescale.

One of Freescale's recommended workarounds is to set a hardware breakpoint, which disables the branch-folding behavior. On PowerPC 7xx processors, the probe sets a hardware breakpoint as long as the **disable_swbp** option is set to `off`.

Locked Data Cache Not Supported on PowerPC 4xx Targets

The probe does not currently support locked data cache. It is possible to set up locked cache lines with no memory backing them, and this is fully supported by the hardware, but the probe does not properly handle this situation with the current firmware. This configuration will be supported in a future release.

Corrupted Registers When Setting an Execute Hardware Breakpoint on Some PowerPC Cores

Registers on PowerPC 8343, 8347, 8349, 8358, and 8360 cores may become corrupted if you set an execute hardware breakpoint that has a range which includes the next instruction to be executed.

Register Definitions Require Setting MULTI Variables

Version 3.8.2 of the probe firmware includes full register support for three PowerPC targets: P2020, MPC8536, and MPC8569. The addresses of all peripheral registers on these targets are offset relative to the CCSR base address. To enable MULTI to read these peripheral registers, you must define the CCSR base address using the following MULTI variables:

```
eval $E500_CCSRBAR_IS_SET=1
eval $E500_CCSRBAR= CCSR_base_address
```

Similarly, for MPC8541, MPC8543, MPC8545, MPC8547, MPC8548, MPC855, and MPC8560, you must set the following MULTI variables:

```
eval $MULTI_PPC_QUICC_CCSR_IMMR_BASE_IS_SET = 1
eval $MULTI_PPC_QUICC_CCSR_IMMR_BASE = CCSR_base_address
```

We recommend adding these lines to an **.mbs** or **.rc** script that you use to debug your target. These lines are already present in the included **.mbs** scripts.

External Trace Trigger In Not Supported on PowerPC 405 Targets

External trace triggers sent to the probe's **Trigger In** port are not supported on PowerPC 405 targets at this time.

Modifying Trigger Settings on PowerPC 4xx Targets

Trigger settings on PowerPC 4xx targets cannot be modified unless the target is halted. If you modify these settings while the target is running, the change is deferred until you halt the target. If you enable trace while the target is running, triggering is not active until you halt and resume the target. No warning or error is issued.

MPC564xC z0 Core Does Not Emit Trace Data on Single Step

While the MPC564xC z0 core supports trace, it does not emit trace data when the target is stepped. If you perform an instruction step on a load or store, no trace data is collected for that instruction.

Nexus Trace Does Not Support Read- or Write-Only Triggers

Nexus trace supports read/write triggers that trigger on a read or write, but it does not support read-only triggers or write-only triggers.

Nexus e200 MDO Width Limitations

For e200 targets that support parallel Nexus trace, check your target documentation to determine supported MDO widths for your specific chip package. 16-bit widths are only supported with the TraceEverywhere trace pod.

MPC55xx and MPC56xx Trace Only Supports One Core at a Time

On multi-core Nexus e200 targets in the MPC55xx and MPC56xx series, you can only trace one core at a time. By default, the probe traces core 0. To trace the second core, connect to **mpserv** using the **-force_trace_coreid 1** option and run your setup script on the core you want to trace. For example, if you have multiple executables to download to your target:

1. In the MULTI Debugger, select the core you want to trace.
2. Use the **load** command to run the script on the core.
3. Select each additional core and use the **load -nosetup** command to prepare it.

If you have a single executable:

1. In the MULTI Debugger, select the core you want to trace.
2. Use the **prepare_target** command to prepare all cores.

After all cores are prepared, resume the target to begin your debugging session.

Single Stepping Over `mtspr dbrrwr, rn` May Not Execute As Expected on QorIQ P4040 and P4080

When the **edm** option is set to `off`, single-stepping over a `mtspr dbrrwr, rn` instruction may not execute as expected. The `dbrr` bits may not be updated. To work around this issue, avoid single-stepping over or setting breakpoints on `mtspr dbrrwr, rn` instructions.

Triggers Are Not Supported on the e200z0 Core of the MPC564xC

Triggers are not supported on the e200z0 core of the MPC564xC processor.

Unexpected Machine Check On 567xR and 567xF

On 567xR and 567xF processors, if a target hits a software breakpoint within 7 non-branch instructions preceding an opcode that is expected to cause a machine check interrupt, the interrupt may occur even if, prior to resuming, the target state is changed so that the machine check condition is no longer met. To work around this issue, place your software breakpoint at least 8 instructions before any opcodes expected to cause machine checks.

Trace Limitations with Stalling Enabled on MPC5777M e200z7 Cores

When the **Stall Processor to Avoid Overflows** trace option is enabled on an MPC5777M e200z7 core, trace data may be corrupted if trace is enabled or disabled while the core is running. Always halt an MPC5777M e200z7 core before enabling or disabling trace, or disable stalling.

Incorrect Trace Decoding on MPC5748G Processors

Tracing more than two cores of an MPC5748G processor may result in corrupted data, which can manifest as either trace errors or the continual overflow of trace data. If you encounter this issue, you must reset the processor to resume correct trace behavior. The only means of preventing this problem is to never trace more than two cores simultaneously.

Incorrect Trace Decoding on MPC5777M Processors

If branch history mode is disabled while tracing an e200z7 core of an MPC5777M processor, and the PC is changed while in debug mode, then one or more instructions in the Trace List may be wrong after the target is resumed. This does not occur with branch history enabled, or with the e200z4 core. This issue is being investigated with Freescale.

Incorrect Trace Decoding on MPC577xK Processors

If branch history mode is disabled, and more than one core on an MPC577xK processor is being traced, there may be an occasional corrupt trace packet that results in trace errors. This does not occur with branch history enabled. This issue is being investigated with Freescale.

Example T4240QDS Setup Script Should Not Be Canceled

If using MULTI 6, do not cancel execution of the example T4240QDS setup script provided by the stand-alone New Project Wizard. Instead, wait for the script to run to completion.

Multi-Core Debug Limitations on QorIQ P3041

In rare cases, running certain multi-core applications on the QorIQ P3041 can cause the target to become unresponsive. When this happens, the probe lists the cores' status as `unknown`. To recover from this state, reset the target.

Trace Errata on Certain P4080/P4040 Silicon Revisions

Early silicon revisions of the P4080 and P4040 contain errata that can cause significant corruption of trace data. Affected silicon is identified by a major revision value of 1 or 2 in the SVR register.

Examples of affected SVR values:

- P4080: `svr=0x82080010` or `svr=0x82080020`
- P4040: `svr=0x82090010` or `svr=0x82090020`

Use P4080/P4040 silicon with major revision 3 or greater to avoid this issue.

Incorrect Trace Data on NXP QorIQ Processors with e500mc and e5500 Cores

If **Branch and Link Correlation Messages** is enabled, there are rare cases in which QorIQ processors may omit an entire trace message. This will usually cause a trace

error, such as "Trace data indicates a branch is taken but there is no branch to take." To work around this issue, disable **Branch and Link Correlation Messages**.

In a separate issue specific to the e5500 family, QorIQ processors may emit a packet with incorrect trace data. If a FIFO overflow occurs just prior to the error, you can reduce this occurrence by taking steps such as tracing fewer cores or enabling **Stall Processor to Avoid Overflows**. When tracing multiple cores, incorrect trace data may occur even without a FIFO overflow. In this case, taking the same steps to reduce overflows may still reduce or eliminate errors.

Trigger Immediately Fails to Trigger After Retrieval

When using **Trigger Immediately** on PowerPC 4xx, the trigger will only be re-armed after halting and resuming the target. If you set up **Trigger Immediately** and resume, you will get one trace download from the immediate trigger. No automatic trigger or download will happen until the target halts and resumes again.

MPC5668 Stalls with Certain Trace Settings

The MPC5668 may stall indefinitely when **Stall Processor to Avoid Overflows** is enabled. If this happens, try turning off stalling, then resume the processor.

Trace Limitations and Stalling on MPC574xB/C/G

The MPC574xB/C/G may stall indefinitely when **Stall Processor to Avoid Overflows** is enabled. When disabled, trigger packets may be missing from the trace data. If you observe either behavior, consider using other settings.

Stalling on MPC5748G z210 Cores

When the **Stall Processor to Avoid Overflows** trace option is enabled on an MPC5748G z210 core, the core may stall indefinitely. In addition, the target may fail to halt. If this happens, try using the **jr** command and re-enabling trace. If the problem persists, consider using other settings.

Debugging SMP Applications Without OSA

When debugging a PowerPC SMP application that does not support OSA, we recommend disabling MULTI's **Auto Check Coherency** debug setting.

Incorrect HSST Trace with Overflows on 57xx and 58xx

On 57xx and 58xx targets using HSST, the processor may emit incorrect packets around a FIFO overflow. If a trace with FIFO overflows contains errors, you can reduce the number of errors by taking steps such as tracing fewer cores or enabling Stall Processor to Avoid Overflows.

x86 Known Issues

Execute Hardware Breakpoints Cannot Exceed One Byte

Execute hardware breakpoints on x86 are always one byte, even if a larger range is requested. The breakpoint will be placed at the first byte of the requested address range.

x86 TraceEverywhere Adapters Not Supported with TraceEverywhere Trace Pod

The current hardware revisions of x86 TraceEverywhere adapters are not supported with the TraceEverywhere trace pod. An updated revision of these adapters will be available in the future.

Probe Cannot Configure Memory Mapping

The probe expects that your target already has a 32-bit or 64-bit flat memory mapping configured; it cannot create this mapping on its own. 16-bit code segments and segmented memory access are not currently supported.

We recommend that you use a boot loader to initialize your target. For example, a USB stick configured to boot GRUB could quickly boot and initialize your target. For additional information, see *install_dir/target/86/generic/board_info.txt*.

tr Command Does Not Work as Expected on Some x86 Targets

Certain x86 targets require 10-15 seconds to reset. If you are having difficulty when issuing the **tr** command to your target, try increasing the **rst_settle** setting. Some x86 targets cannot perform a precise reset at all, and must perform a running reset using the **tr r** command instead.

MULTI Reports Any x86 Processor as a Pentium Pro

When connecting to your target with MULTI, MULTI will report the CPU as a Pentium Pro. MULTI does not have settings for newer processors at this time. If your target is 64-bit, MULTI will report the CPU as x64 instead.

Cannot Write to Segment or Table Registers

The segment registers and table registers are currently read-only.

Simultaneous Run-Mode and Freeze-Mode INTEGRITY Debugging Is Not Supported

Simultaneous debug of INTEGRITY via run-mode (**rtserv**) and freeze-mode (**mpserv**) is not supported at this time. Use the **enable_debug** setting to specify whether the probe or the target handles debug exceptions.

You can set freeze-mode software breakpoints on newer processors like Sandy Bridge and Apollo Lake without having any effect on run-mode debugging. Doing so still requires an appropriate setting for the **enable_debug** option.

INTEGRITY run-mode partnering is not currently supported on x86 targets.

Halt and Breakpoints on Sandy Bridge Targets Is Synchronous

The halt feature and breakpoints on Sandy Bridge are synchronous. When halting or breaking on any one core using the probe, all cores on the target halt, including cores that are not configured in the JTAG scan chain. It is not possible to halt one Sandy Bridge core and leave other cores running. The resume feature is not a synchronous operation by default. Halting a core halts all cores, but resuming that

core may not resume the other cores. Synchronous resume is possible using the **MULTI groupaction** command, or the probe's **gc** command.

Running Programs that Change Address Mappings

To download and run a program that changes address mappings (such as an INTEGRITY kernel) on an x86 target, use the **-load_physical** option when connecting to your target. When using this option, you will not be able to set software breakpoints in your code until the address translation mapping is enabled, but hardware breakpoints will work. To work around this issue, set a hardware breakpoint that resets all software breakpoints shortly after the kernel starts running.

For example, if you are using INTEGRITY, you can set a hardware breakpoint by adding the following lines to your **.mbs** or **.rc** setup script:

```
configure continuePlaybackFileOnError on
hardbrk execute __ghs_ind_crt0 { Tog q off ; Tog q on ; resume }
configure continuePlaybackFileOnError off
```

This hardware breakpoint allows you to set software breakpoints before downloading your program. You can manually remove it during your debugging session if you need to use the hardware breakpoint slot that it occupies. If you do not remove the breakpoint and you run the program multiple times without reloading it, MULTI will warn you that this breakpoint is already set. You can ignore this warning.

If you need MULTI to handle system calls, use the **-hwbpssc** option when connecting to your target to use a hardware breakpoint to catch system calls.

Software Breakpoints in SMP Debugging

Software breakpoints are now supported in an SMP environment if you specify the **-synccores** argument when connecting with **mpserv**.

Booting a Multi-Core Target After Reset

Targets with Intel x86 processors typically have a BIOS check that prevents them from completing their boot sequence unless all cores are running. Be sure to resume all cores after a reset to allow for the BIOS to complete its startup sequence.

Booting a Multi-Core OS Clears Hardware Breakpoints on Secondary Cores

When any core is reset on an x86 target, hardware breakpoints set on that core are cleared. After the core begins to boot, you can halt it and set hardware breakpoints. Because booting a multi-core OS (such as INTEGRITY) on an SMP system causes secondary cores to go through a reset sequence, you should set hardware breakpoints on these cores after booting the OS.

Target Halts in System Management Mode Code

Some x86 targets enable system management mode (SMM). If SMM is enabled and you halt the target, it may halt in SMM code. If you did not intend to debug SMM code, resume the target and try halting again.

When SMM is enabled, the **vc** and **vrh** diagnostics may fail.

Nehalem-Based Target Cannot Leave System Management Mode

Some Nehalem-based targets have a BIOS that performs a processor coherency check while in system management mode (SMM). This check asserts if any of the processors are not running. This may happen while debugging the system via JTAG if one core is halted while the others run. One of the running cores may assert, which causes the system to remain in SMM until restart. In this case, you may see a printed assertion in **SmmDispatcher.c**. To avoid this assert, halt and resume all cores simultaneously using the group run and group halt commands (see the documentation about legacy methods of group execution and control in the *MULTI: Debugging* book). On such systems, software breakpoints and hardware breakpoints will probably not work, because they only halt one core. Synchronous breakpoints will be supported in a future firmware version.

